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A DISCRETE LATERAL POSITION PROSTHETIC EYE CONTROLLER

BY

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DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

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The undersigned certify they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled A DISCRETE LATERAL POSITION PROSTHETIC EYE CONTROLLER submitted by TODD PAUL SHEPEL in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE.

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Abstract

A customized non-invasive discrete lateral position prosthetic eye controller is described. Current technologies and physiological considerations are reviewed to place this controller in context. Careful selection of hardware components addresses the cosmetic concerns of the design. Hardware is designed to track the lateral position of the human eye. Position tracking activates a servomotor and results in a controlled bi-directional stepped lateral pivot of the prosthesis about the vertical axis of its rotation. The controller is described at the electronics and control signal level. Simulation results are presented to validate the choice of components for the design considerations of the new controller. Conclusions are drawn and future research possibilities are recommended.

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1. Introduction

Our eyes are a marvelous organ that allow us to appreciate the beauty of the world we live in, to read and gain knowledge, and to communicate our thoughts and desires to each other through visual expression. Vision is the most fundamental of our senses and it is perhaps the greatest tragedy of all when blindness takes this modality away. Typically the eyes work together when viewing environmental objects [Weber, 1971]. Muscles turn the eyes in all directions and keep the eyes parallel with each other. The natural synchronous parallel positioning of the eyes is a feature of human physiology that goes without notice when the eye muscles are in perfect working order. When an individual looses an eye, there are many adjustments that the individual will make. The individual must adapt physically and mentally to mono-ocular vision. Emotionally, the individual and the people close to the individual must learn to accept the condition. Normally, each eyeball is held in position in the orbital cavity by various ligaments, muscles and fascial expansions that surround it (see Figure 1.1). Inserted into the sclera are three pairs of muscles, two pairs of rectus muscles orthogonal to each other and one pair of oblique muscles

angled as the name implies, obliquely. These muscles, named extraocular muscles move the eyeball in the orbits. These eyeball movements allow you to focus an image on the central retina. If the muscles of the eye are without serious damage, these muscles can be re-attached to a prosthetic eye. In terms of outward appearance, the individual will appear to have close to normal eye movement. The objective of this research addresses the cosmetic concern of lateral eye movement after reconstructive prosthetic eye surgery, when normal eye movement via traditional methods is not possible.

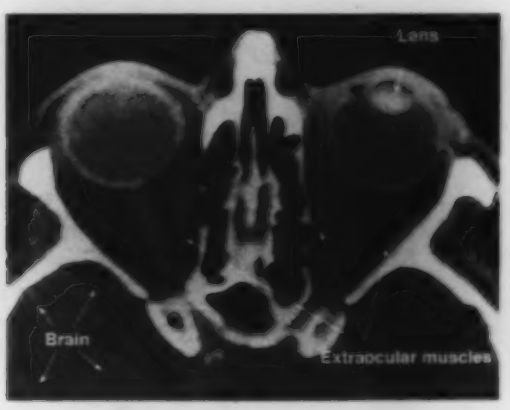


Figure 1.1 Cross-section of optical region

In 1997 the Electrical Engineering - Advanced Robotics and Tele-operations group and a mechanical engineering group began working with the Craniofacial Osseointegration

and Maxillofacial Prosthetic Rehabilitation Unit (COMPRU) of the Misercordia Hospital in the design of a prosthetic eye controller. Originally, the intent of the group was to create a prosthetic eye controller that would detect the eye blink and track the horizontal and vertical positions of a natural eye. The tracked information would then, in real time, update the position of actuators within the socket of a prosthetic eye. The group decided that the design required that the controller be unobtrusive and non-invasive.

Upon reviewing the spatial dimensions of an eviscerated ocular orbit, the group sought to find actuators small enough to fit within this cavity. It was quickly decided that there was only enough space for a single actuator. This, and the need to show progress in the design, limited the scope of the design to tracking and updating the eye position in only the horizontal (lateral) direction.

Currently, no controllers are commercially available which are easily adapted to perform the tracking and encoding of the eye position. Custom controller hardware had to be developed to complete the prosthetic eye controller design requirements. A micro-controller would readily perform the logic functions intrinsic to eye

tracking. Unfortunately, a micro-controller requires a large amount of supporting circuitry to convert analog sensor input into a form that a micro-controller can use. This extra circuitry alone begs the question of "what is unobtrusive?" Ultimately, the decision to minimize circuit size and complexity results in a simple design that compromises output resolution for the gain in a reduction of circuit size. The prosthetic eye controller hardware design implements six digital / mixed integrated circuit packages, two capacitors, four photodiode, four resistors, two diodes, and one, four resistor, resistive network to perform the operations required to track a natural eye and actuate a prosthetic eye.

The system block diagram of the prosthetic controller is described in Figure 1.2. The block diagram identifies the major components within the eye position tracking system. The variables are defined as:

$x_1(t)$: Position of the biological eye as measured by the photodiode sensors at a sample time.

$x_2(t)$: Position of the prosthetic eye at a sample time.

$e(t)$: error between $x_1(t)$ and $x_2(t)$ at a sample time.

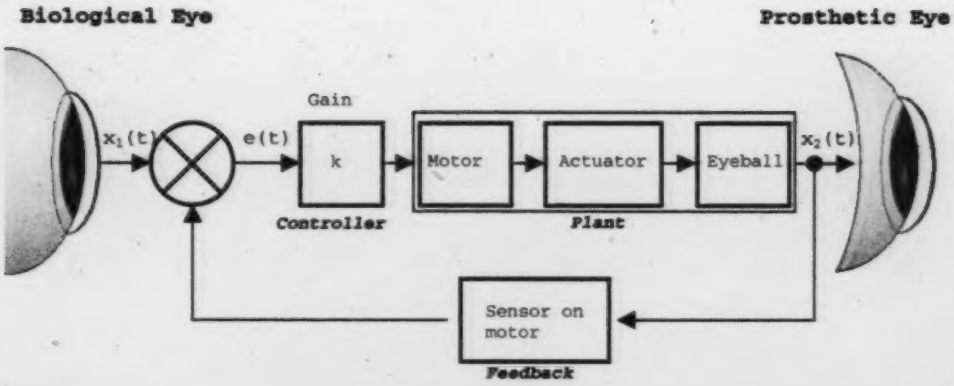


Figure 1.2 System Block Diagram of Prosthetic Controller

The servo controller moves the motor, the actuator and the prosthetic eye to a new position $x_2(t)$ based on information present within a pulse-width encoded position signal $x_1(t)$. The error in position is measured by a rotation sensor present on the servomotor and produces a feedback signal $e(t) = x_1(t) - x_2(t)$. The error signal is fed back into the controller to stabilize the position error in the plant output.

The prosthetic eye controller performs lateral eye tracking by sensing light reflected within the natural eye. Light reflected from the pupil, iris and the sclera [Figure 1.3] is collected by four photodiode detectors mounted on a pair of glasses worn by the individual. In real-time, the controller determines and encodes the pupil position. The encoded information updates an actuator via a servomotor.

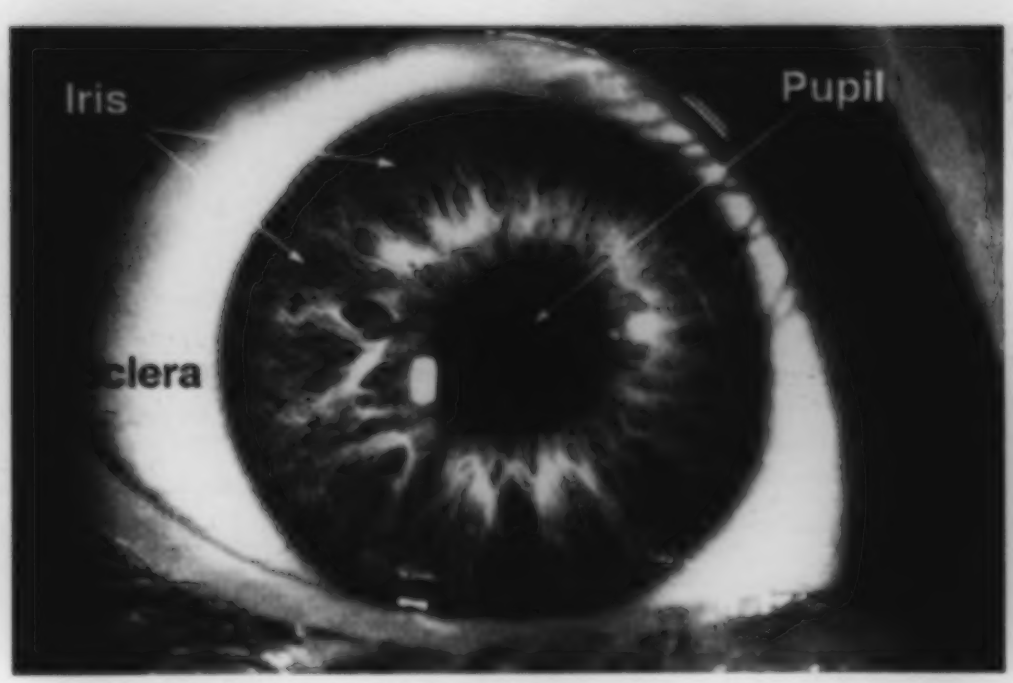


Figure 1.3 The pupil, iris and the sclera

The thesis is divided into several chapters. Chapter 2 gives an overview of the history of prosthetic eye applications, eye position sensor technology and optical physiology. In chapter 3, a detailed description of the design of controller hardware for the project is presented. In chapter 4, details of the simulation of controller operation and the experimental results are presented. Chapter 5 gives conclusion for the design and makes suggestions for future research. A netlist of the spice design is included as an appendix to the thesis.

2. Literature Review

The literate review consists of a history of the artificial eye, a detailed study of sensor methods applicable to the study of eye movement, an optical physiology section and optics section, details of the eye metrics and eye movements. These diverse sections form the foundation upon which this thesis is based.

2.1 History of the Artificial Eye

Since the beginning of medicine, physicians have been using their senses to determine various physical parameters of patients. In an attempt to quantify the measurement of these parameters from a living system, there has been an increase of technology to applications of clinical and biomedical research. Instruments that were developed originally for the physical sciences have since been adapted for specific medical applications. This engineering adaptation is the focus of this thesis, with the introduction of a solid-state optical prosthetic lateral position controller.

Fifty years ago, an ophthalmic plastic surgeon was virtually unknown. Anaplastology was in its infancy. A solid-state optical prosthetic control system was

unimaginable. An ophthalmologist would enucleate the eye and dismiss the patient forever, considering with the removal of the eye, their responsibility was concluded. The problem of developing an optical prosthesis in an enucleated orbit has challenged physicians since Cleobury introduced the procedure in 1826. It remained for Mules in 1885 to use a glass sphere as an implant in the eviscerated eye and then two years later for Frost and Lang to insert one into Tenon's capsule [Iverson, et al., 1973]. These pioneers made the first significant contributions to the modern prosthetic eye.

After World War II and the Korean War, a new breed of ophthalmologists, plastic surgeons and ocularists came to the foreground. They were not satisfied with the accomplishments of the past and endeavored to gain better cosmetic results. .Using modern technology and new materials, further major advancements have been made by inventive surgeons and skilled ocularists. Ligaments have been attached to artificial eyes to allow the artificial eye a slight mobility [Culler, 1972]. New pioneers are now taking on the phenomenal task of completely restoring lost vision due to any number of visual impairments. There is much work to complete to obtain this end. This leaves a wide technology gap between a relatively simple non-

functional prosthesis and the next generation of seeing optical prosthetics.

Today, it is a standard procedure for an ophthalmic plastic surgeon to perform prosthetic eye restoration. Depending upon the patient's condition and the surgical reconstruction requirements, this restoration is generally completely cosmetic. Research contained within this thesis reduces the technology gap by adding a lateral tracking function to the prosthesis. Today this functionality is only cosmetic, however in the future this functionality will be a necessary condition for a seeing prosthesis.

2.2 Survey of Eye Sensor Methods.

There are many means by which the position of the eye may be tracked [Young, 1975]. In 1975, Young presented a good description of eye tracking methods and paradigms. Since 1975, new technology has been introduced. This new technology enhances the same tracking paradigms. The lateral eye tracking application addressed within this thesis has two prerequisites. The prerequisites effectively eliminate most previous eye tracking methods, however the procedural paradigms are still valid. Ultimately, the sensing method employed is a hybrid of an infrared photo detector and a simple CCD array.

The first prerequisite requires that the sensor and controller be discrete. Discrete means small in size, unobtrusive and self-contained. A number of researchers [Tock et al. 1996, Nakano et al. 1996, and Yoshida et al. 1995] worked on methods of sensing driver drowsiness. These researchers used a camera method to track to eyelid separation. A camera is not a valid option for this research. A patient having undergone orbital surgery is sensitive to their appearance. Indeed this research is intended to better naturalize the appearance of one with an ocular prosthesis.

The second prerequisite requires that the sensor and controller be non-invasive. The application of a micro-electronic system to a biological system can be a highly complex undertaking. The origin of these complexities stem from the incompatibilities of biological tissue [Dario et. al., 1995]. A non-invasive approach eliminates the microelectronics system / biological system interfacing issues. Researchers [Gupta, et al. 1996, Varri et al., 1996, Häkkinen et al. 1993 and Berg et al. 1991] used forehead Electro-OculoGraphy (EOG), ElectroMyography (EMG) and Electro-EncephelaloGraphy (EEG) signals to detect eye movements and blinks. These methods have many advantages, especially in regard to being discrete. However, the

concern with keeping the sensor and controller non-invasive and cosmetically pleasing does not allow these approaches to be exploited at this time.

Magnetic blink detectors have been designed to detect when a blink takes place. Consideration of the blink is beyond the scope of this research, however the applicability of the blink to general eye movement is important. Blink research lends to a better understanding of the eye physiology. Takagi uses an amorphous wire magneto inductive displacement sensor to detect slight changes in eyelid position [Takagi et al. 1994]. Sonoda detects eyelid vibrations by fixing a small magnetic disk to the eyelids. Using a magnetometer sensor slight eyelid movements are detected [Sonoda 1992]. Hirano describes how a micro pressure chip taped to the eyelid detects the eye blink [Hirano et al. 1995]. These methods, while somewhat more discrete, would also need to be invasive if the cosmetic considerations were truly important.

Charge Coupled Device (CCD) image detectors have been explored by several researchers; There are too many to explore here. These CCD have many generic and specific applications. The governing principles are as applicable to eye position detection as image detection of anything else. While a CCD is attractive in its potential for computed

position resolution, is not practical simply because too much computing support technology is required. A simplified infrared photodiode sensor array, combined with digital logic, achieves the CCD benefits of a wider range of movement and improved stability.

2.3 Optical Physiology

To understand the application of how photodiode sensors are able to measure light reflected from within the eye, it is necessary to study the various elements between the light source and the retina. In general, the structures met by the light on the passage to the eye are seen in Figure 2.3.1. These include: the anterior surface of the cornea, the substance of the cornea, the posterior surface of the cornea, the aqueous humour, the anterior surface of the lens, the substance of the lens, the posterior surface of the lens and the vitreous humour. This application requires analysis of the cornea, aqueous humour, and anterior surfaces of the lens, and iris.

The complex optical system can be reduced to the basis of a simple system by the application of the principles of the theorem of Gauss, provided the components of which it is formed are centered on the same optical axis. The eye forms, approximately, such a homocentric system.

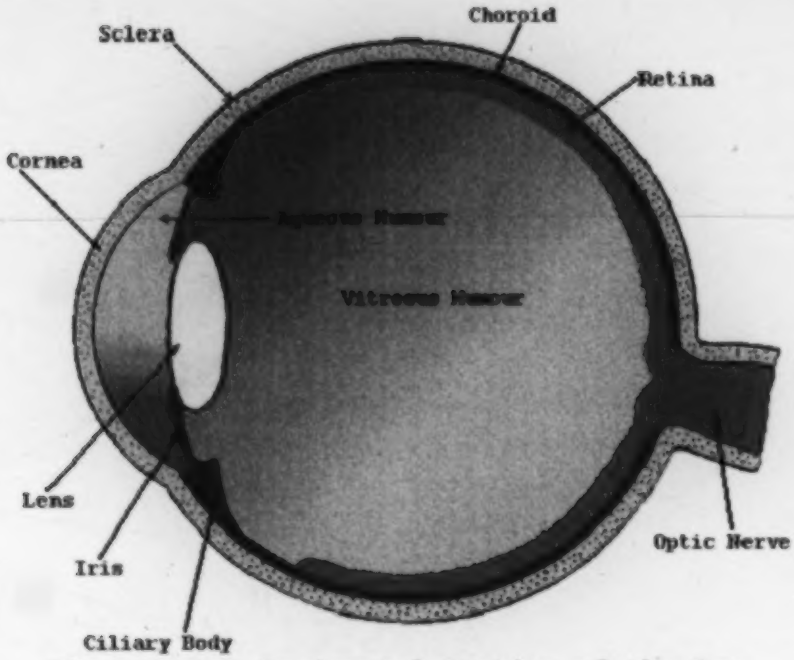


Figure 2.3.1 Horizontal Section of the Eye

We find its cardinal points to be as in Figure 2.3.2. The analysis of the reduced eye is referred to as *the schematic eye* [Gullstrand, 1911]. Some of Gullstrand's measurements are outlined in Table 2.3.3. References to the cardinal points of the eye and Gullstrand's measurements serve as a guideline for determining sensor orientation and position. The analysis can be made simpler when we notice that the two principal points and the nodal points are very close together. There is no great inaccuracy if for each pair, an intermediate point is substituted. This concept is referred to as *the reduced eye* [Donders, 1866].

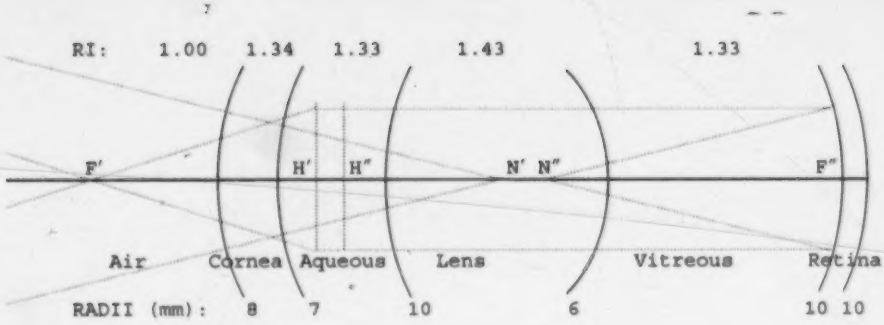


Figure 2.3.2 Cardinal points of the eye.

F', the anterior principal focus, 15.7 mm in front of cornea.
F", the posterior principal focus, 24.13 mm behind the cornea, upon the retina.
H', H", the principal points in the anterior chamber.
N', N", the nodal points, in the posterior of the lens. The refractive indices are approximate.

Table 2.3.3 Gullstrand's #1 Schematic Eye

	Unaccommodated	Max Accommodation
Refractive Index		
Cornea	1.376	1.376
Aqueous & Vitreous	1.336	1.336
Lens	1.386	1.386
Equivalent Core Lens	1.406	1.406
Position (mm)		
Anterior Corneal Surface	0.0	0.0
Posterior Corneal Surface	+0.5	+0.5
Anterior Lens Surface	+3.6	+3.2
Posterior Lens Surface	+7.2	+7.2
Radius of Curvature (mm)		
Anterior Corneal Surface	+7.7	+7.7
Posterior Corneal Surface	+6.8	+6.8
Anterior Lens Surface	+10.0	+5.33
Posterior Lens Surface	-6.0	-5.33

2.4 Optical Power Transfer

The analysis of light transmission through the eye is an important exercise simply because this analysis establishes the limitations of the photodiode sensor measurement system. As the thesis results are based upon the theoretical operation of the circuit, these limitations are of interest. The limitations are due to the physical constraints of the eye, the ambient light level and the sensor sensitivity. In practice, measuring sensor response to various light conditions begs establishing its theoretical limitations due to all influencing factors.

A spectrum of light enters the eye from the subject's environment. Sunlight consists of approximately 43% infrared radiation, 13% ultraviolet radiation, and 44% visible light. Artificial light sources have there own spectrums but virtually all visible light sources emit some near infrared radiation. Ultraviolet light is almost entirely absorbed within the cornea, while the ocular media transmits about 90% of near infrared and visible (400nm~1400nm) wavelengths to the retina [Pitts, et al., 1993]. Light passes from the air, through the cornea, into the aqueous, and through the lens. When measured alone, 87% of an 875nm monochromatic source is transmitted through the cornea [Freegard, 1998]. The aqueous humour shows

absorption bands at 908nm, 1320nm, and 1453nm. Clearly, a near infrared source with its spectral density centered about 875nm will pass through the outer eye relatively unaffected.

Light transmission in the outer eye is of interest when referring to the power coupling of a particular optical path. Most literature specifically states the amount of light transmitted to the retina of the eye [Davson H. 1990, Benedek 1971, Boettnet 1962, Geeraets 1960, Ludvig et al. 1938 and Duke-Elder 1932]. In this study, it is of interest to know the amount of light reflected at the pupil, the iris, and the sclera. The pupil is the lens window which allows light to enter the inner eye (eyeball). The iris is a circular disk of colored muscle lending itself to eye color. The sclera is simply the white of the eye. Even more importantly, knowing how much of this light is transmitted back into the environment is paramount. Using Fresnel's law, [Marcuse, 1977] and literature gathered on ocular transparency, the mathematics of determining the ratio of reflected light to incident light is not difficult. These values are to some degree dependant upon the moisture of the eye, the specific refractive indexes and specific absorption characteristics of the eye mediums. Eq. 2.4.1 allows the calculation of

the ratio of reflected light to incident light between adjacent mediums. If absorption is overlooked, the light not reflected is transmitted. Eq. 2.4.2 determines the percent of transmitted light to the incident light.

$$\text{Eq. 2.4.1} \qquad \%\,Reflected = \left(\frac{\eta_1 - \eta_0}{\eta_1 + \eta_0}\right)^2 \cdot 100\%$$

$$Eq\ 2.4.2 \qquad \%Transmitted = \left[1 - \left(\frac{\eta_1 - \eta_0}{\eta_1 + \eta_0}\right)^2\right] \cdot 100\%$$

Where:

η_0 $\triangleq$ refractive index of incident medium

η_1 $\triangleq$ refractive index of new medium

Fresnel's reflection/transmission laws are employed to trace each optical path. The first optical path has the light transmitted from the environment, through the cornea, through the aqueous, reflected off the anterior surface of the lens, back through the aqueous, the cornea and back into the environment. Like the first optical path, the second and third optical paths have the light transmitted from the environment, through the cornea, through the aqueous. The second path requires the calculation of the light reflected on the anterior surface of the iris. The

third optical path requires the calculation of the light reflected on the anterior surface of the sclera. The second and third optical paths also require the calculation of the transmitted light back through the aqueous, the cornea and back into the environment. The completed calculations yield the following results: Approximately 0.02% to 0.05% of the infrared light incident upon the anterior surface of the cornea and reflected at the pupil is transmitted back into the environment. Using a similar calculation, 46% ± 10% of the infrared light incident upon the anterior surface of the cornea and reflected at the iris, is transmitted back into the environment. This wide range of values is largely due to the variation of eye colors. The sclera of the eye transmits greater than 75% of the infrared light incident upon it back to the environment. From these calculations, it is clear that when these reflective surfaces are compared against each other at any specific time, the reflecting surface cannot be mistaken. Only in extremely dark conditions would a photodiode sensor system be mistaken. We know this to be true because when we look into someone's eye, unless it is extremely dark, the boundaries separating the pupil from the iris and the iris from the sclera of the eye are not difficult to ascertain.

2.5 Pupil and Iris

Light entering the eye takes the form of a cone. The base of the cone is formed at the anterior surface of the cornea. The apex of the cone falls somewhere behind the retina. The pupil is an entrance through which the cone of light must pass [Boettner, et al., 1962]. The eye responds to the ambient light intensity by altering the width of the iris. The iris is a concentric colored ring of muscle of a non-fixed width surrounding the pupil. The iris contracts in a reflex response to higher light levels to reduce the diameter of the pupil and, hence, increase the width of the iris. The iris dilates, in a similar reflex manner, in response to low light levels to increase the diameter of the pupil and reduce the width of the iris. Pupil reflex appears to be triggered by cone and rod stimulation [Alpern et al. 1962]. Pupil horizontal diameter ranges from 2mm to 8mm. The iris has an outer ring diameter approximately 13.0mm in diameter and an inner ring diameter equal to that of the pupil diameter. In light conditions, discerning the position of the pupil center may be difficult for the photodiode sensors. Similarly, in dark conditions, the iris may be overrun by the diameter of the pupil. Eq. 2.5.1 and 2.5.2 describe retina size as a function of the light level. These functions are shown in Figure 2.5.3.

- [Moon and Spencer, 1944]:

Eq. 2.5.1 $Diameter = 4.9 - 3 \cdot \tanh(.4 \cdot (\log(L) + 1))$

- [DeGroot & Gebgard 1952]:

Eq. 2.5.2 $Diameter = 10^{.8558 - .000401 (\log L + 8.6)^2}$

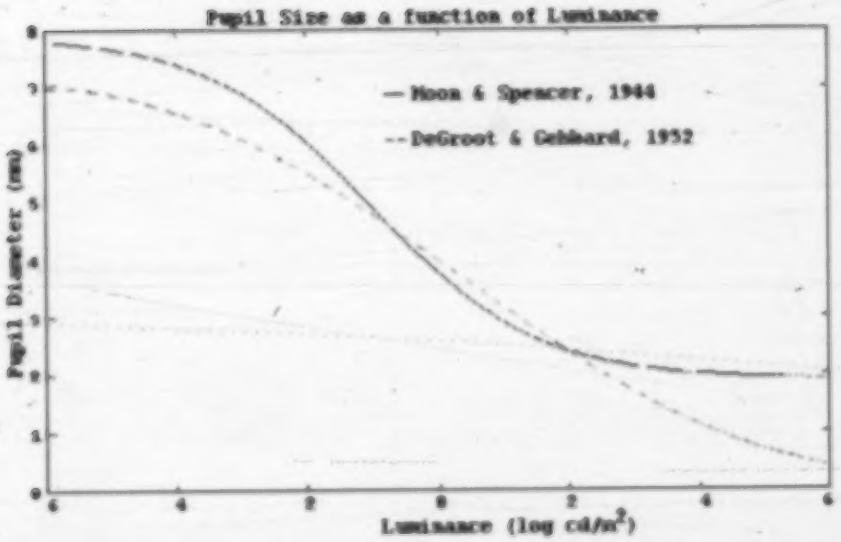


Figure 2.5.3 Pupil Size as a Function of Luminance

2.6 Eye Movement and the Blink

Because the prosthetic eye controller application tracks the position of the biological eye in order update the prosthetic eye position, it is important to understand the movement characteristics of the human eye. The ocular motor system consists of two subsystems: version and vergence. Both of the subsystems are subject to latency. When the eyes move in response to a newly moving target, a 200ms latency proceeds the eye movement [Dell'Osso et al. 1977, Becker 1989 and Fuchs et al. 1985]. This latency establishes a baseline in an acceptable latency between the biological eye and the prosthetic eye. The prosthetic eye should not be perceived as sluggish with respect to the biological eye.

The version and vergence subsystems give rise to three types of eye movements: fast eye movements and slow eye movements from the version subsystem, and vergence eye movements from the vergence subsystem [Dell'Osso et al., 1977]. Fast and slow eye movements are conjugate, while vergence eye movements are disconjugate. Conjugate eye movements adjust the eyes by innervating associated pairs of rectus and/or oblique muscles. This conjugate muscle innervation causes the eyes to take the same angle relative to a very distant object along the optical axis of

rotation. Conjugate eye movements enable the person to track laterally moving objects. Disconjugate eye movements adjust the eyes for different viewing distances in depth. Disconjugate eye movements allow the eye to focus on objects near in proximity.

The stimulus to elicit a fast eye movement is called target displacement. The result is called a voluntary saccade. The velocity varies from 30 to 900 degrees/second and its duration from 30 to 100 or more milliseconds is dependent on the amplitude of the saccade, which varies between 0.5 and 40 degrees of visual angle [Becker 1989 and Fuchs et al. 1985]. The movement is conjugate and ballistic and the control system is discrete. This means that even though there is continuous visual information, motor commands generated are irrevocable. Tracking of fast eye movements by the photodiode sensors can be subject to the largest degree of latency when the eye moves quickly from one corner to the other. The latency will consist of the time actuate the prosthetic eye and the travel time of the prosthesis over the entire lateral range. This will contribute to a sluggish performance of the prosthesis.

Slow eye movements are typically generated while the eye tracks a slow moving target. Eye velocity during slow eye movements is characterized as smooth and is typically

less than 50 degrees/second in either or both of the horizontal or vertical fields. Another type of slow eye movement (not smooth pursuit) results from stimulus causing the head or body to accelerate. The movement is smooth and the velocity may achieve 400 degrees/second.

The stimuli for vergence eye movements are target displacement or target motion toward or away from the subject. The eye velocity is usually less than 20 degrees/second. The eye movement is disconjugate but smooth, and the control is continuous [Weber, et al., 1971]. The photodiode sensors are not able to track vergence eye movements because the eye tracking circuitry is specifically designed to perform only conjugate movement of the prosthesis with respect to the biological eye.

Blinking is normally an involuntary act, but it may also be carried out voluntarily. Blink detection is beyond the scope of this thesis; however, the effect of the blink is important to consider during the operation of the controller. The prosthetic controller system, which does not filter the blink, experiences interference during the blink. Reflex blinking is caused by bright light and by stimuli exciting the fifth corneal cranial nerve. The corneal reflex lasts approximately 100ms. The function of the corneal reflex is to protect the eyeball. In the

waking hours the eyes blink at regular intervals of every two to ten seconds, the actual rate being a characteristic of the individual. The function of this is to spread lacrimal secretions over the cornea. Voluntary blinking allows the individual to control the eyelids by their own accord. The individual may choose the have the eyes remain opened or closed for indefinite periods of time. Voluntary eye movements generally dominate the reflex blink [Davson, 1990].

The literature reviewed, in whole or in part, sets the foundation upon which this thesis is based. The knowledge referenced forms the guiding principles for the design of the optical prosthetic controller. Both the successes and failures are of interest. All of the aforementioned bettered the design in principle, theory of operation and practicality.

3. DESCRIPTION OF PROPOSED CONTROLLER HARDWARE

3.1.1 Design Goals and Methodology

The proposed prosthetic eye controller evolved in a series of specification, prototyping, simulation, and testing phases. The proposed controller will be referred to as the prosthetic eye controller or, simply, the controller. The controller measures, with respect to a fixed reference point, the en vivo lateral position of a human eye. The controller then supplies a continuous signal, containing information about the lateral eye position, to a servomotor circuit.

At the beginning of the project, several technologies related to object tracking, and more specifically eye movement tracking, were researched and their characteristics were identified and evaluated. Photo detection techniques were closely examined to assist in the definition of a sensor subsystem. Using the technical details of the actuator, and the sensor information, an input/output specification for the system was created to design the system hardware.

Features from general circuits were also incorporated into the design. The clock, complete with pulse-width coded modulation, the counter, analog multiplexers,

comparator, and register circuits have specifications that are readily obtained. Circuit function, size, power usage, and simplicity are the primary design considerations. Based on comparisons between movement detection methods and the more important requirement for a non-invasive self-contained design, it was decided that implementing a light sensitive, pupil position detection method would provide the best coverage of the design considerations. Photodiode sensors, the signal conditioning and actuation hardware for the prosthetic eye controller would need to be mounted, discretely, on a pair of glasses. In addition to the aforementioned, availability of a powerful, inexpensive, SPICE mixed signal simulation environment affects the circuitry development cycle and the choice of the components used to design the system hardware. The design is a result of the modeled circuits available within the SPICE package. A standard development platform, Microsoft Windows 95 version 4.00.950a and the Personal Edition of Interactive Image Technologies Ltd., Electronic Workbench version 5.1 (Electronics Workbench) would be the SPICE simulation and design prototyping and testing environment.

It is advantageous to consider this particular circuit design a task in programming. Each digital or mixed signal component has a specific function. Each circuit must

receive input, transform it, and output the processed signal(s) to adjoining circuits.

While the simulation environment is able to provide a solid prototyping environment, the performance of the controller must be critiqued as an operational circuit. The prosthetic eye controller circuit, while never assembled entirely, is thoroughly examined. Sensors and associated circuitry were assembled to gather empirical data. To tune the sensor resistive networks, empirical data, in combination with tabulated reference data and theoretical models, allows an iterative process to converge on the correct resistive values. The analog input is quickly transformed into the digital domain by a comparator. The comparator interface must be extremely sensitive. Much work goes into ensuring parallel input conditions for the photodiode sensors. As much work is done to insure an extra-ordinarily high sensitivity to the most slight differences in the values of the sensor input. Models for several comparators are tested over a full range of input conditions. Once the context of the comparator signal enters the digital domain, the SPICE environment shines in the analysis and simulation of the design. Performance of the prosthetic controller simulation and the

results of the experimentation are documented for a variety of operational conditions within section 4.

3.1.2 Description of Circuits

In measurement systems the functions of timing, signal transduction, signal conditioning, processing, and output are not always divided into physically distinct blocks. The border between signal conditioning and processing is somewhat indistinct. Generally, there is a need for some signal processing of the sensor output signal before its end use. Some authors use the quickly becoming stale generic term "interface" to refer to signal modifying elements that change signals from one data domain to another. The design operates in two data domains. There is an analog input data domain and a digital processing and output data domain. A data domain is the name of a quantity used to represent or transmit information. The concept of data domains and conversion between domains is very useful to describe sensors and electronic circuits associated with sensors (Malmstadt, et al., 1981). In the case of the proposed prosthetic eye controller system, the comparator circuit acts as an interface; transforming the analog input signals into a digital signal. Similarly, but

less distinct interfaces are present within the clock, the analog multiplexers, the counter and the register circuits.

In the analog data domain information is carried by signal amplitude (voltage). The analog data domain is prone to electric interference. The choice of sensors and signal conditioning requires a special degree of care. In the digital data domain signals have only two values (ON or OFF). Information is contained in encoded serial and parallel words.

Figure 3.1.2.1 is a block diagram describing the sub-circuits present within the prosthetic eye controller. The operational control of the controller begins and ends with the clock. The clock sends a continuous repeating series of ON and OFF pulses to the counter and register circuits. These clock pulses initiate state transitions within the counter circuit and cause the counter to output an incrementing address with each state transition. The counter output value sets the input address of the first analog multiplexer (MUX1). The analog multiplexer is a four input to one output switch. The address of MUX1 sets which sensor channel's analog value is sent to the negative terminal of the comparator. As stated previously, the comparator transforms analog signals from two respective sensor channels into a digital value. The comparator

element is the "one decision" brain of the controller. If the output voltage value from the sensor channel activated on MUX1 is less than the output voltage value from the sensor channel activated on MUX2, then the comparator output will enable the register to load the output value of the counter. If the output voltage value from the sensor channel activated on MUX1 is greater than the output voltage value from the sensor channel activated on MUX2, then the comparator output will inhibit the register and the previous register value persist. As stated, the register obtains a new value whenever the analog value of the counter sensor is less than the analog value of the register sensor. The register digital value sets the input address of the second analog multiplexer. The analog multiplexer is a four input to one output switch. The input address of MUX2 sets which sensor channel's analog value is sent to the positive comparator terminal.

The comparator and the entire prosthetic eye control system operates in real-time, continuously comparing combinations of two of four sensor channels, attempting to determine which sensor resistor has the lowest output DC voltage. A low DC output voltage is associated with a darker region such as the pupil. The register is always updated with the address for the sensor channel having the

lowest DC voltage. The register address update is completed each 20ms.

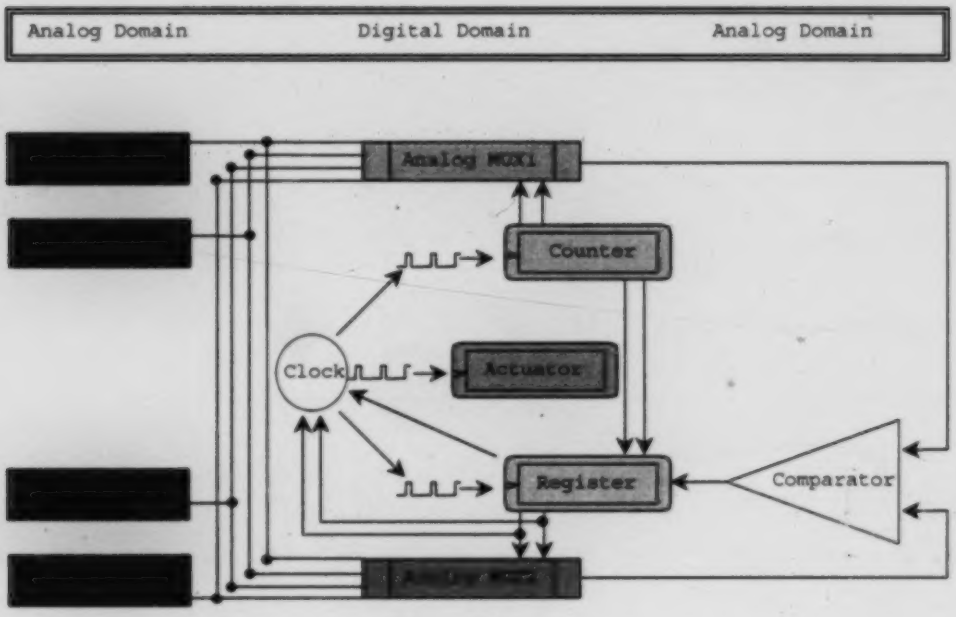


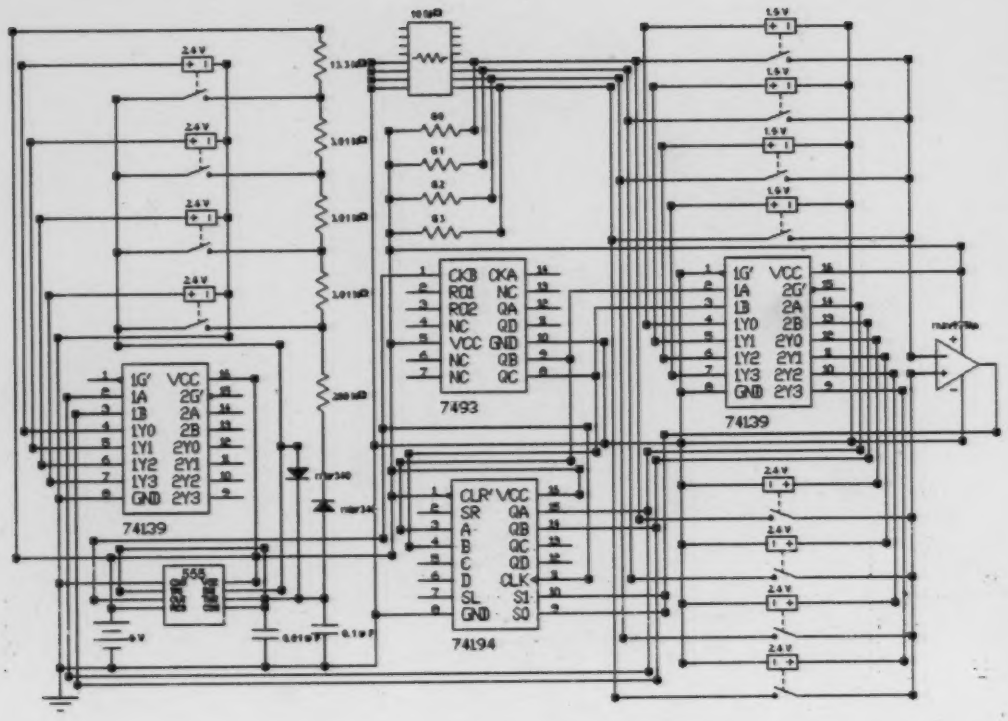
Figure 3.1.2.1 Block Diagram - Prosthetic Eye Controller

3.1.3 Prosthetic Eye Controller Schematic

The layout of the entire circuit in the final construction of the controller is of great importance for its end use. Obtaining the components and constructing such a precise concealed device requires a considerable amount of IC engineering, fabrication engineering, and VSLI

design knowledge. While the components required to construct a prototype controller are readily available, the concealed, tight integration of all of the components requires a considerable investment of time and money. In addition, the tools necessary to complete this work are not readily obtained, and even if these tools could be obtained, time would need to be spent learning how to use these tools. As VLSI design and fabrication are not the focus of my research, the time cost benefit ratio is high. For these reasons the controller is not constructed. A larger prototype would be possible to construct; however, due to a shortage of time, completion of this thesis takes priority over the completion of a prototype. Preparation of such a prototype is not feasible at this time. The preparation of a prototype will require obtaining the specified devices. Testing and tuning the circuits and analyzing the results.

Figure 3.1.3.1 illustrates the model of the prosthetic eye controller. The model is not intended to portray the board level layout of the controller. Its function serves only as an operational model of the controller. The Electronics Workbench SPICE simulator is shipped with a predetermined number and type of models, and this limits the modeling, simulation and analysis.



University of Alberta - Department of Electrical Engineering.	
Title Model of Lateral Position Prosthetic Eye Controller	
Document Number Figure 3.1.3.1	Rev 1.0
Drawn By Todd Paul Shepel	Date August 8, 1998

The Electronics Workbench package apparently has some ability to import other models and device types, after several such attempts, this exercise proved fruitless. Models for the analog multiplexers and photodiode sensors were simulated with combinations of models available within the SPICE package. The schematic models the photodiode sensors as resistors (S0-S3) and models the analog multiplexers as voltage switches and encoders. Section 4 covers the details on the validity of the model replacement. The netlist of the schematic may be found in the Appendix.

The remainder of section 3 covers details of the sub-circuits contained within the controller. These sub-circuits include the power supply and voltage regulator in section 3.2.1. Information about the sensor sub-system is discussed in section 3.2.2. Information about the clock design and functionality are discussed in section 3.2.3. Section 3.2.4 and 3.2.5 cover the details of the counter and the counter analog multiplexer, respectively. Sections 3.2.6 and 3.2.7 go over the details of the register and register analog multiplexer, respectively. The comparator is discussed in section 3.2.8. Finally, the actuation of the servomotor by the pulse width coded clock signal is discussed in section 3.2.9.

3.2.1 Power Supply and Voltage Regulator Circuit

3.2.1.1 Power Supply and Voltage Regulator Introduction

A voltage regulator integrated circuit and two capacitors are connected as a $+5V_{DC}$ voltage regulator circuit. A single $+9V_{DC}$ alkaline battery is the input to the voltage regulator. The control circuitry, the control signals and the servomotor are supplied with a continuous $+5V_{DC}$ regulated source.

3.2.1.2 Power Supply

As previously stated, the actual design of a market ready prosthetic controller requires the tight integration of the controller components. The battery is perhaps the most difficult component to effectively reduce in size and therefore conceal. There are several batteries available in the marketplace that can fit the power requirements for the design of the controller and servomotor. That is, less the dimensional aspects. The bottom line in the selection of a power supply is as follows: The amount of charge that a battery is able to supply is proportional to the battery volume. A voltage that exists between battery terminals is dependent upon the chemical reactions that take place within the battery. Electrodes react with an electrolytic

paste surrounding the electrodes when the battery terminals are connected through some resistive load. The resistive load allows the flow of charge from the resulting chemical reactions. Chemical reactions between the electrodes and the paste render the resulting chemical compounds spent. The time which a battery can supply a current is determined solely by the number of available chemical reactions. Available chemical reactions are a combination of reactive electrode surface area and the availability of reactive chemicals (electrolytic paste). The amount of reactive chemicals and electrode surface area is dependent upon the battery volume.

Ultimately, the choice of batteries will be a compromise between reduced battery size and operational lifetime. For the servomotor, this compromise is a very important design concern. If a battery is chosen which will fit into the optical cavity, thereby eliminating the need to expose external connecting leads, this battery would likely occupy the bulk by the optical cavity and would have to be replaced and/or recharging frequently. If the servomotor is connected with wires to an external supply, hiding these connectors becomes the challenge. Hiding the connector leads is the most reasonable option. If the wire is thin in diameter, short in length, and of

the right color, the leads will blend into the background of the skin. Figure 3.2.1.2.1 illustrates how to effectively hide the external wires from sight. The illustration shows three leads. One lead is for power ($+5V_{DC}$), the second is an actuator signal lead, and the third is for the ground.

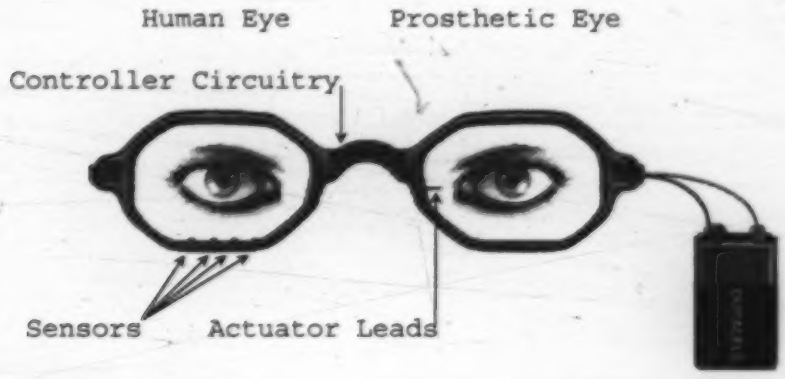


Figure 3.2.1.2.1 Front view of glasses with sensors, and external leads.

The maximum power that the controller and the servomotor use should be the guidelines in the selection of an electric cell. The power dissipated within the controller is determined by summing the individual integrated circuit power dissipation. Table 3.2.1.2.2 outlines the power dissipation for each circuit element. The servomotor's nominal voltage is $+5V_{DC}$ with load current 120mA.

A simple Duracell alkaline $+9V_{DC}$ dry cell, while not exactly state of the art or readily hidden on a pair of glasses, is the battery that this design will refer to. The Duracell $9V_{DC}$ alkaline battery supplies 560mAh. If the prosthetic eye were to scan back and forth continuously for over the lifetime of the battery, the prosthetic eye would remain operational for approximately 278 minutes.

Table 3.2.1.2.2 Circuit Supply Currents

#	Circuit Element	$V_{NOMINAL}$ (V)	Current (μA)
1	Servomotor	5.0	120000
1	Voltage regulator	5.0	20
4	Photodiode sensor	1.8	43
1	Timer	5.0	170
1	Counter	5.0	300
1	MAX analog multiplexer	5.0	10
1	ADG analog multiplexer	5.0	2
1	Register	5.0	200
1	Comparator	5.0	300
	Control signals	5.0	≈200
	Discrete components	5.0	≈100
	Total:		121600

3.2.1.3 Voltage Regulators Design

The 78LM05AC series of fixed positive voltage regulators are complete $+5V_{DC}$ regulators fabricated on a single silicon chip. The regulator has an operating temperature range from 0°C to +125°C. The devices are available in three standard transistor packages. The 78LMXX series of regulators are available in a three lead, metal TO-39 package, a TO-92 plastic package and the

plastic SO-B package. The TO-92 package is the most suitable choice for this application. In any case, the 78LM05AC regulator can deliver output currents in excess of 100mA if adequate heat sinking is provided. If internal power dissipation is too high, the internal thermal shutdown circuit prevents the IC from overheating. Power dissipation for the 78LM05AC is internally limited to be less than 750mW. Regulator stability is achieved by methods that provide very good rejection of load or line transients as seen with TTL logic. A recommended minimum load capacitance of 0.01µF is required to limit high frequency noise. A value of 0.10µF is used within the design. While the regulator is not located more than three inches from the battery input, an input capacitance of 0.33µF is used to allow for circuit alterations which would require regulator schematic changes. Figure 3.2.1.3.1 illustrates the regulator used within the prosthetic design.

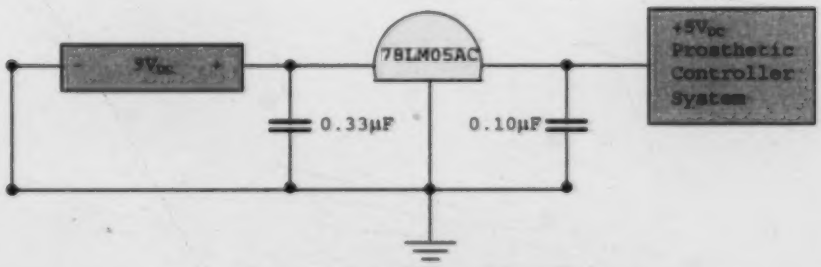


Figure 3.2.1.3.1 Voltage Regulator

3.2.2 Infrared Photodiode Sensors

3.2.2.1 Sensor Introduction

Photodiode sensors form the interface connecting the measured system to the controller system. This interface communicates the lateral position of the eye, with respect to a fixed reference measurement system, via light affected by the position of the eye. A spectrum of light from the environment enters the eye through the cornea and travels through the interior of the eye. A portion of the light is reflected at the pupil, the iris or sclera. This reflected light is the affected light measured by the fixed reference measurement system. When looking into the eye of the subject, what is seen is the light reflected at the pupil, the iris and sclera as seen in figure 1.2. In much the same way, a photodiode sensor detects the same reflected light. The boundaries that separate the pupil from the iris, and the iris from the sclera, can be measured in terms of contrast. These boundaries of contrast are even more pronounced to infrared photodiode sensors. This is because near infrared light is not absorbed by the substances of the outer eye to the extent which visible light is. Light incident upon a photodiode is measured indirectly. A photodiode sensor produces an output voltage

that is a function of the incoming radiation intensity. The sensor voltage is the transduced light characteristic applied within the controller.

3.2.2.2 Sensor Design

After reviewing and taking into consideration several eye position-sensing alternatives, the sensing method offering the most desirable characteristics for the prosthetic controller application happened to be a subminiature near-infrared photodiode sensor. Four Hewlett-Packard HSDL 5420 infrared 7.5ns PIN photodiode detectors are referred to within the design. Hewlett-Packard HSDL 5420 SMT photodiode detector packages are small enough to go virtually unnoticed on a pair of glasses. Dimensions of the detectors are $2mm^2$ by 3mm in height. The measurement system is considered fixed with respect to the horizontal (lateral) rotational axis of the eye. Each sensor is mounted on the lower portion of the glasses. The sensors are directed just below the equator, toward a point just above the intersection of the horizontal and vertical rotational axes of the eye, slightly offset by a fixed angular displacement of 15°. The result is a distinct set of focal coordinates along the equator of a surface consisting of the anterior surface of

the lens, the anterior surface of the iris and the sclera. Figure 3.2.2.2.1 and 3.2.2.2.2 illustrate the sensor orientation with respect to the eyeball.

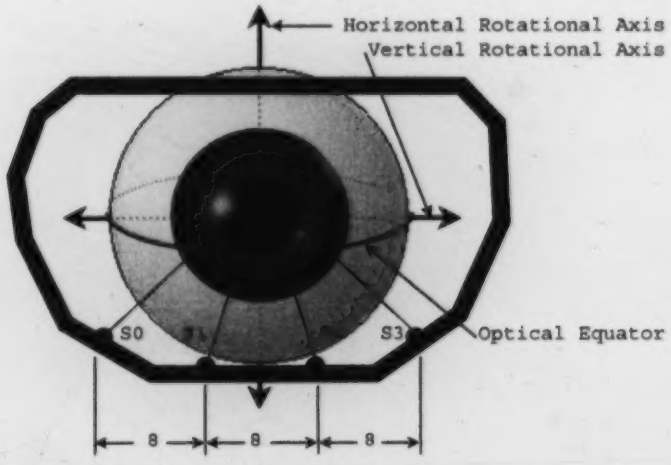


Figure 3.2.2.2.1 Portrait Photodiode Sensor Placement Dimensions in mm.

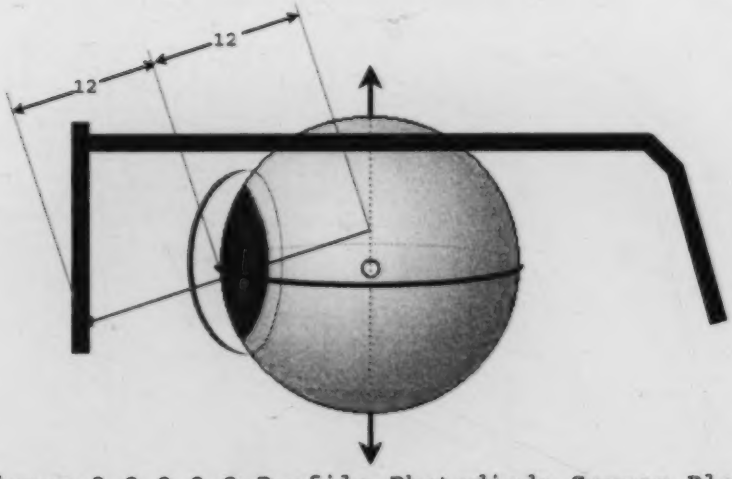


Figure 3.2.2.2.2 Profile Photodiode Sensor Placement Dimensions in mm.

Each sensor can be fixed to the lower rim of the glasses with plastic glue. The photodiode detectors are sensitive to near infrared light falling within 14° of either side normal to the sensor optical centerline. The sensors are spaced 8.0mm apart. An 8.0mm horizontal spacing gives each sensor an independent region of light selectivity for 87% of the light content when the sensors are 16mm distant from the anterior surface of the cornea.

A pair of glasses will tend to slide up and down the nose to some extent. The region of light selectivity overlaps more significantly when the sensors are moved beyond 16mm from the anterior surface of the cornea. When the sensors are 24mm from the anterior surface of the cornea, approximately 37% of the light content is shared between adjacent sensors. Ideally if the glasses were fixed permanently on the face, with respect to the human eye, the sensor system would function optimally.

The sensor system is designed to compare the light intensity at two independent coordinates. More exactly, of four independent sensor coordinates, combinations of two coordinates are compared sequentially. The detectors are sensitive to light with a spectral center at 875nm and a spectral bandwidth between 770nm and 1000nm. When the internal photoelectric effect occurs in a photodiode

detector, it is possible to obtain a voltage that is a function of the incoming near infrared radiation intensity. The photovoltaic effect in the *p-n* junction of a photodiode sensor is caused by the increased width of the depletion region when a reverse bias voltage is applied to the photodiode.

The photodiode detectors are continuously enabled. Voltages appear across the sensors at all times. The counter and register analog multiplexers perform the switching resulting in the comparison between sensor voltages. All eye movements affect the photodiode measurements. Unfortunately, included within all eye movements is the eye blink. If the sensor channels are compared during an eye blink, the result of the comparison will be of no value to the prosthetic controller. In fact, the result is analogous to interference and affects the stability of the prosthetic output. At this time, there is no means by which to filter how the eye blink affects the controller output. Biological eye motion in the vertical direction adversely displaces the pupil and increases the likelihood of photodiode sensors incorrectly determining the lateral position of the pupil.

Anchoring the detectors to the lower quadrant of the glasses helps to reduce the effects of the eye blink. The

lower eyelid is displaced to a lesser degree than the upper eyelid during an eye blink. In addition to this, the lower eyelashes typically have a shorter length than the upper eyelashes. By mounting the sensors on the lower quadrant of the rim, there is a direct unobstructed optical path between the equator of the eye and the receptive surface of the sensor most of the time. This is clearly more advantageous than having the sensors mounted on the upper part of the glasses when the long upper eyelashes can block the optical path even when the eyes are fully open. Mounting the sensors on the base of the glasses serves one other important engineering perspective. Typically light sources are more prevalent from above in both natural and artificial light settings. Because light is reflected at an angle negative to the incident angle with respect to a line normal to the reflecting surface, the vast majority of the reflected light is directed at and detected by sensors mounted on the lower quadrant of the glasses.

3.2.2.3 Input Resistive Network

The photodiode detectors create currents relative to the detected infrared light obtained within the photosensitive regions of the reflecting eye surface. The current creates a voltage across the resistor (R_L) that is a

linear function of the near infrared light detected by the sensor. The output voltage (V_0) is strictly linearly related to the incident flux intensity (Φ) when the photodiodes are connected in a reverse biased fashion. This means that a simple resistive value can be chosen to limit the current flowing through the photodiode and provide the maximum range of output voltages across the photodiode. A model, as seen in Figure 3.2.2.3.1, best describes the Hewlett-Packard HSDL 5420 photodiode.

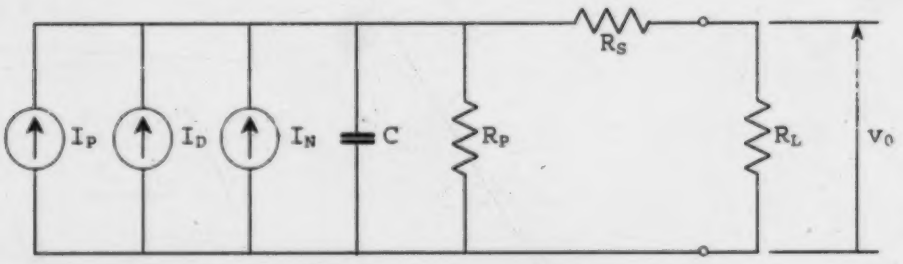


Figure 3.2.2.3.1 Photodiode equivalent circuit. I_P is the signal current; I_D is the leakage current, I_N is the total noise current; R_P is the dynamic resistance; C is the diode capacitance; R_S is the series resistance; R_L is the load resistance.

If the effect of noise current is neglected, the characteristics of photodiode operation are described in the following equations:

$$Eq.\ 3.2.2.3.1 \qquad V_0 = (I_P + I_D) \cdot \frac{R_L \cdot R_P}{R_L + R_P + R_S}$$

The inverse current sources are

$$Eq.\ 3.2.2.3.2 \qquad I_P = \alpha \cdot q \cdot \Phi \cdot A$$

$$Eq.\ 3.2.2.3.3 \qquad I_D = I_0 \cdot \left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

Where

α	Δ	Quantum yield for the detector
q	Δ	Charge on an electron
Φ	Δ	Incident flux intensity
A	Δ	Detector area
I_0	Δ	Inverse saturation current
V	Δ	Voltage applied to the diode
k	Δ	Boltsmann's constant
T	Δ	Absolute temperature

The photodiode resistor values were chosen after experimental testing. A resistive value of approximately 1MΩ seems to provide a good output range over a full range of lighting conditions. Each photodiode detector is connected in a reverse biased manner to a 1MΩ resistive value. A 4 x 1MΩ resistive-network slightly reduces the size of circuit. Photodiode operation as a function of the ambient radiation and the distance between the reflecting surface and the sensor is covered in section 4.1. Section 4.2 covers the simulation of the modeling of the photodiode within the Electronics Workbench SPICE package. The resistive value of the detector decreases with increased light intensity. Similarly, with reduced light intensity, the detector resistance increases. The output of the input resistive network is the voltage measured across the 1MΩ resistor. The resistive output voltage changes in direct proportion to the light intensity. Figure 3.2.2.3.2 illustrates the photodiode resistive network circuit and its connection to the prosthetic eye controller circuit.

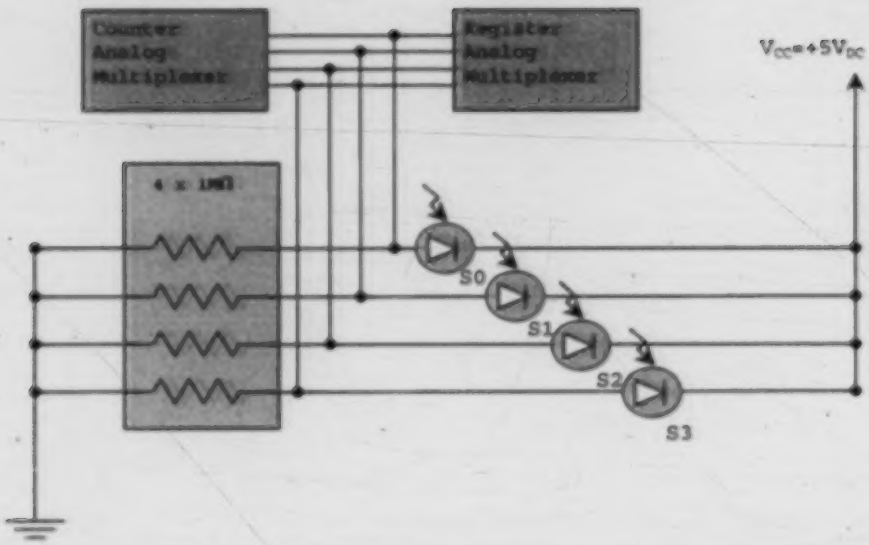


Figure 3.2.2.3.2 Photodiode Resistive Network

3.2.3 Clock Circuit

3.2.3.1 Clock Introduction

A timer integrated circuit, an analog multiplexer, five resistors, two capacitors, and two diodes are connected as a self-triggering monostable multivibrator circuit with a discrete variable pulse-width coded modulated output. The clock output signal provides the actuator input and provides the time slicing functionality within the prosthetic eye controller. It is henceforth referred to as the clock. The clock output is connected to the counter, the register and the actuator. Output from the clock triggers state changes within the counter and register circuits. The clock is also designed to update the position of the artificial eye, via the information present within the pulse-width coded modulated signal. New position information updates the actuator as frequently as every 20ms (50 updates per second). In a worst case scenario, the position update can take as long as 80ms and the true position may be incorrect by one sensor position. This update analysis assumes the velocity of the eye is less than the speed at which the sensors are scanned. Clock output characteristics include a 20.23ms ± 0.04ms period with a discrete variable duty cycle. The pulse

width takes one of four values: 1.0ms, 1.2ms, 1.5ms, or 1.7ms. Logic levels alternate between logic "1" ($+5V_{DC}$) and logic "0" ($0V_{DC}$), where logic "1" is the pulse width.

3.2.3.2 Clock Design

The clock has two functions. The first function is to provide output in the way of a pulse-width coded modulated signal to the servomotor electronics. The second function is to provide the time slicing functionality within the digital domain of the controller. For both functions, the timer facilitates the necessary signals. With externally connected resistors, capacitors, diodes and an analog switch, this device operates as a discrete variable duty cycle pulse-width coded modulated circuit. Physical characteristics including the IC package dimensions, numbers of pins, power usage and thermal limits are considered when selecting each component. The Texas Instruments TCL555ID LinCMOS timer is available in an eight pin, 3.0mm by 6.4mm, small outline "D" type package as well as a "Y" type 50 by 64 mil chip. This package operates between -40°C and +85°C with a $+5V_{DC}$ supply voltage, and consumes 725mW of power below +25°C.

The Analog Devices ADG609 analog multiplexer operates with a single $+3V_{DC}$ or $+5V_{DC}$ supply and is available in a ten

pin, 6mm x 5mm TSSOP package, with a power dissipation of 1.5μW below +70°C. The design is connected to use the $+5V_{DC}$ voltage supply. The ADG609 is not available in a chip form. Three precision 3.01kΩ, one 13.3kΩ and one 280kΩ metal resistors are chosen with a 125mW MIL power rating at +70°C. Two Motorola MBR340 Schottky barrier rectifiers have the fast switching, low forward voltage, and reverse saturation current required to maintain the correct clock period and duty cycles. The diodes are highly temperature sensitive. To maintain the 20ms clock period to within 10%, the diodes must operate between 0°C and +38°C, ultimately limiting the upper and lower thermal limitations of the controller. Two radial lead tantalum capacitors of values 0.10μF and 0.10μF are chosen to complete the timer circuit. The capacitors are rated to 50Watts and can withstand a $+60V_{DC}$ surge between -55°C and +125°C.

Both the counter and register circuits trigger positive or negative transitions via clocked flip-flops. While it is a common practice to synchronize the operation of all flip-flops by a common clock or pulse generator, this design requires that the counter and register change state on negative and positive clock edges respectively. When a clock is used, all flip-flops that change state do

so in response to the clock pulse rather than in response to some other input signal. The clock is the state change trigger within the prosthetic eye controller circuit.

The clock design uses all of the features of the TCL555 timer integrated circuit. Figure 3.2.3.2.2 illustrates the connection of the clock circuit and the supporting/output circuits. The correct selection of supporting analog components is based upon the equations that govern the clock operation. From equation 3.2.3.2.1, equations 3.2.3.2.1, 3.2.3.2.3 and 3.2.3.2.4 are produced. Where V_{CC} = $+5V_{DC}$, the initial voltage across the capacitor is $E_{CI} = 2/3V_{CC}$, and the final voltage across the capacitor is $E_{CF} = 1/3V_{CC}$. τ_T is the period of the waveform; τ_{NC} is the time to charge the capacitor to its final value; and τ_{ND} is the time to discharge the capacitor to its initial value. Parameter N takes a value of 1, 2, 3 or 4, depending on the digital input to the clock analog multiplexer.

Eq. 3.2.3.2.1 $$\tau_T = \sum_{i=1}^{5} R_i \cdot C \cdot ln\left[\frac{V_{CC} - E_{CI}}{V_{CC} - E_{CF}}\right]$$

Eq. 3.2.3.2.2 $$\tau_T = \sum_{i=1}^{5} R_i \cdot C \cdot \ln 2$$

Eq. 3.2.3.2.3 $$\tau_{NC} = \sum_{i=1}^{N} R_i \cdot C \cdot \ln 2$$

Eq. 3.2.3.2.4 $$\tau_{ND} = \sum_{i=N+1}^{5} R_i \cdot C \cdot ln\, 2$$

It should be noted that the capacitor current should be much larger than both the trigger current and the threshold current. Small capacitors are affected by stray capacitance and the high resistance pickup of unwanted noise spikes. A capacitor with too large a value can decrease the accuracy of the timer periodicity calculation due to a relatively long ramp up/down time. Ideally, the clock waveform period is 20ms with duty cycles of 1.0ms, 1.2ms, 1.4ms or 1.6ms. The simulated results, including the actual periods and duty cycles are outlined in section 4.2. The capacitor is somewhat arbitrarily set to a standard value of 0.100μF. Using equation 3.2.3.2.2, the sum of the resistors, one through five, is determined.

Values of the five resistors are specific to the requirements of the servomotor electronics. There is a more detailed analysis of the actuator circuit in section 3.2.9, but it is important to state the clock output characteristics (the input requirements of the actuator) at this time. One of four characteristic waveforms is sent to the actuator. The waveform sent is dependant upon which one of the four sensors detects the pupil position. The characteristics of these waveforms are depicted in Figures 3.2.3.2.1.a through 3.2.3.2.1.d.

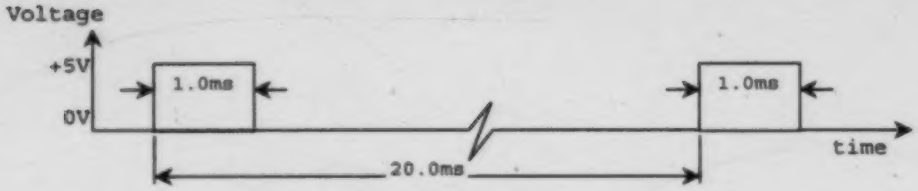


Figure 3.2.3.2.1.a Ideal Clock Pulse Width Modulated Out 00

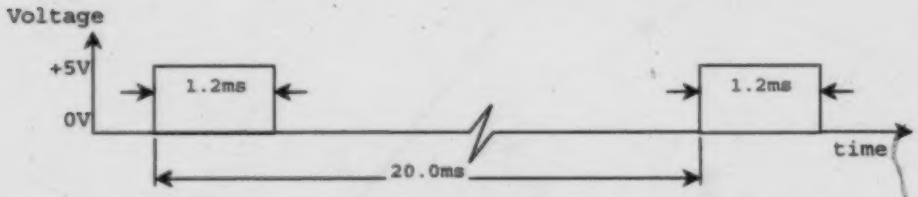


Figure 3.2.3.2.1.b Ideal Clock Pulse Width Modulated Out 01

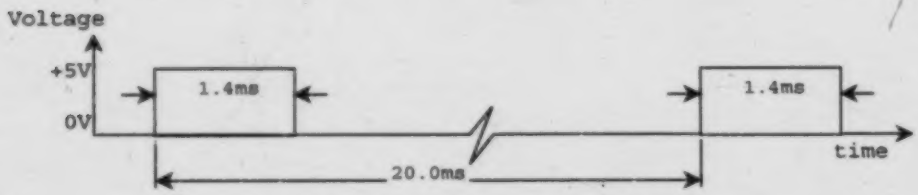


Figure 3.2.3.2.1.c Ideal Clock Pulse Width Modulated Out 10

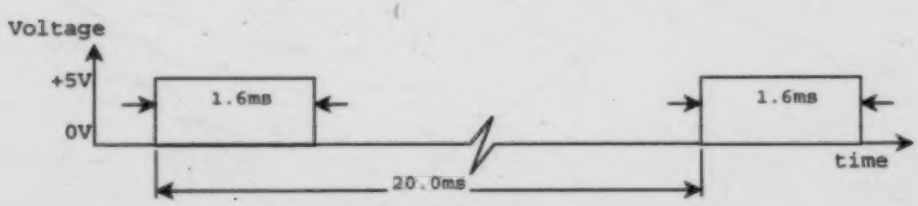


Figure 3.2.3.2.1.d Ideal Clock Pulse Width Modulated Out 11

Using equation 3.2.3.2.3, parameter R_1 is determined by setting N=1 and τ_{NC}=0.10ms. Similarly, parameter R_2 is determined by setting N=2 and τ_{NC}=0.12ms. The result is the sum of R_1 and R_2. Parameter R_3 is determined by setting N=3 and τ_{NC}=0.14ms. The result is the sum of R_1, R_2 and R_3.

Parameter R_4 is determined by setting N=4 and τ_{NC}=0.16ms The result is the sum of R_1, R_2, R_3 and R_4. Parameter R_5 is obtained by subtracting the sum of R_1, R_2, R_3 and R_4 from the total resistance obtained in Eq. 3.2.3.2.2.

A time of 20ms is required to sample any one sensor. One sensor sample interval fits into a single update interval and updates the actuator each 20ms. A 10ms time lag between exists between when the when the human eye moves and when the resulting signal is sent to the actuator. This lag is a necessary result of exploiting a single timer integrated circuit as a multiple operation device. Two timers could also be used. A timer with a 20ms period could update the servomotor and a second timer with a sub-20ms period could provide the time slicing functionality. A decision was made to prioritize a reduced circuit size at the cost of a 10ms actuation lag.

The selection of a diode is not simple. In fact the necessary use of diodes within the circuit complicates the design. The diodes allow the clock circuit to have a duty cycle less than 50%. Diodes inherently have a non-linear voltage current relationship and are highly temperature sensitive. Diode selection is based upon the exhibition of the correct time average current when in the forward biased condition at an ambient temperature of +27°C. The Motorola

MBR340 Schottky barrier rectifier has a fast switching characteristic, a low forward voltage and the reverse saturation current (≅72μA) necessary to produce the correct time average current within the clock circuit. With use of circuit simulation package, the resistors are scaled up by 5% over the calculated value. Tuning the clock circuit in this way corrects the clock operation for the non-linear performance of the diodes.

Upon completing the calculation of resistor values, taking into consideration the non-linear diode operation, and simulating the operation of the clock circuit, the following 1% tolerance standard value resistors and capacitors are established:

R_1 ≙ 13.3kΩ

R_2 ≙ 3.01kΩ

R_3 ≙ 3.01kΩ

R_4 ≙ 3.01kΩ

R_5 ≙ 280kΩ

C_1 ≙ 0.10μF

C_2 ≙ 0.01μF

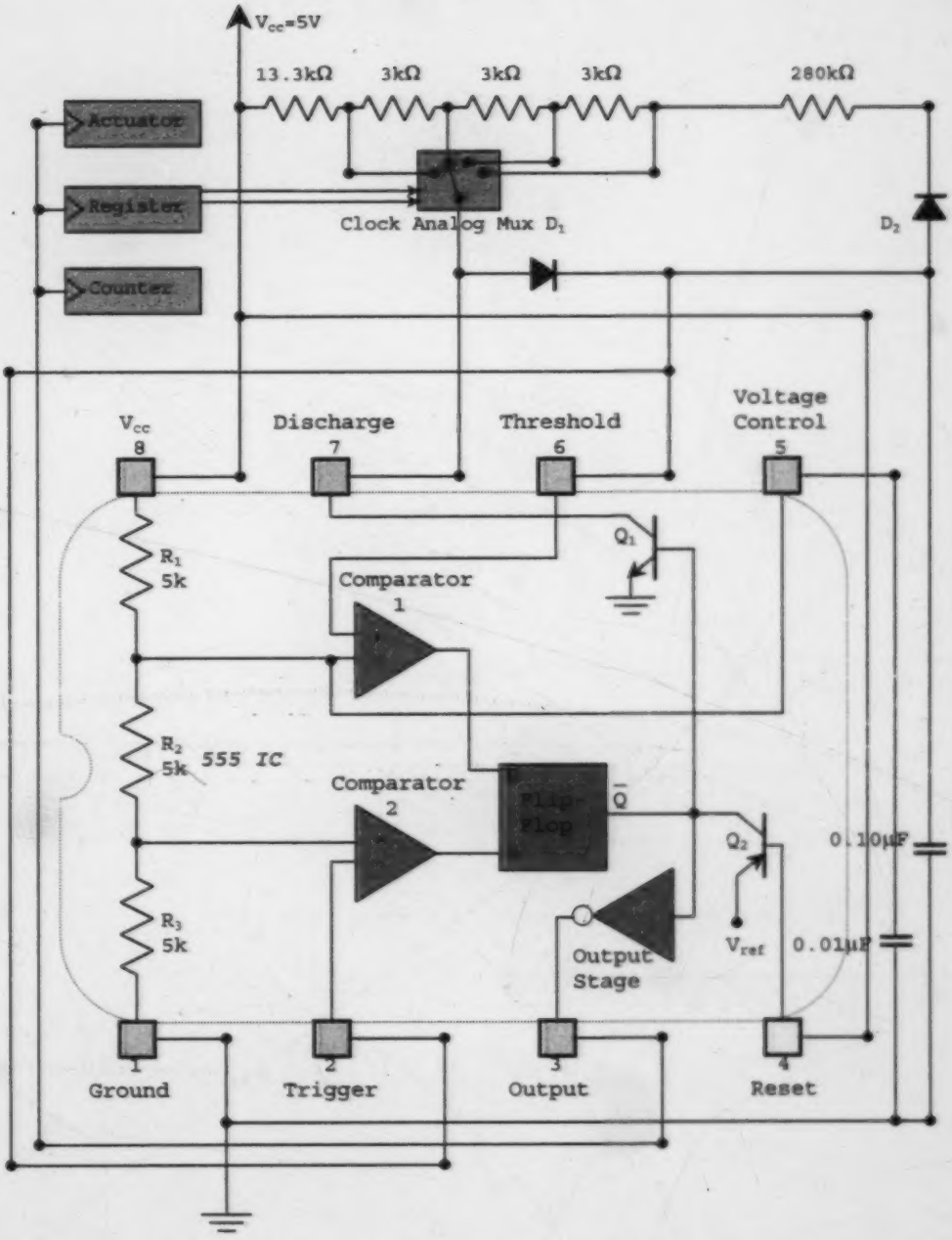


Figure 3.2.3.2.2 Clock Circuit Diagram

3.2.3.3 Clock Analog Multiplexer Circuit

The analog multiplexer switches one of four differential analog inputs to a common differential output depending on the state of the register output connected to terminals ADDRA and ADDRB and an enabling input (INH). Each of the two sets of differential inputs and outputs are completely independent of each other, except in the respect of which switches are open or closed. A differential input/output pair is implemented as the clock analog multiplexer circuit. The second differential input/output pair is implemented as the register analog multiplexer. As stated, the control of these switches is provided by the register output. The ADG609 decoder actuates four switches. Each voltage-controlled switch has one of two positions. A switch can be opened or closed. The decoder closes the voltage-controlled switch that corresponds to the input and opens the other three switches. The closed switch is shorted to the common lead.

The register value changes each time a new photodiode sensor, receives less reflected light than the previous registered photodiode sensor channel. The least light is reflected from the surface of the lens (pupil). When the new photodiode is receiving less light than the previously registered photodiode channel, the register changes state.

The register analog multiplexer may never change state if the registered photodiode sensor channel is continuously receiving the less light than the other photodiodes.

Figure 3.2.3.3.1 shows the complete clock analog multiplexer, its digital and analog inputs and its common output. The output of the register is connected directly to the digital inputs of the clock analog multiplexer. The least significant bit of the register is connected to the ADDA terminal of the multiplexer. The most significant bit of the register is connected to the ADDB terminal of the multiplexer. The digital inputs (ADDA and ADDB) on the ADG609 analog multiplexer serve as switch address references. The digital enable (INH) input of the register analog multiplexer is permanently connected to the $+5V_{DC}$ voltage supply reference, perpetually enabling the differential switch. Each analog input (NO0 through NO3) of the clock analog multiplexer is connected to a node between two resistors in the series of resistors which charge/discharge the clock capacitor. The negative terminals of the switches are connected to a common output (COM). The common analog output (COM) is connected to the clock discharge terminal. Resistive values R_1, R_2, R_3, R_4 and R_5 when connected in series produce four nodes. Each of the analog inputs NO0, NO1, NO2 and NO3 are connected at

the four nodes R_{12}, R_{23}, R_{34}, R_{45} respectively. Depending upon which switch is closed, the clock output duty cycle is the sum of resistor values up to the closed switch, divided by the total resistance. The result is a fixed period pulse train with a variable duty cycle dependent upon the register address value.

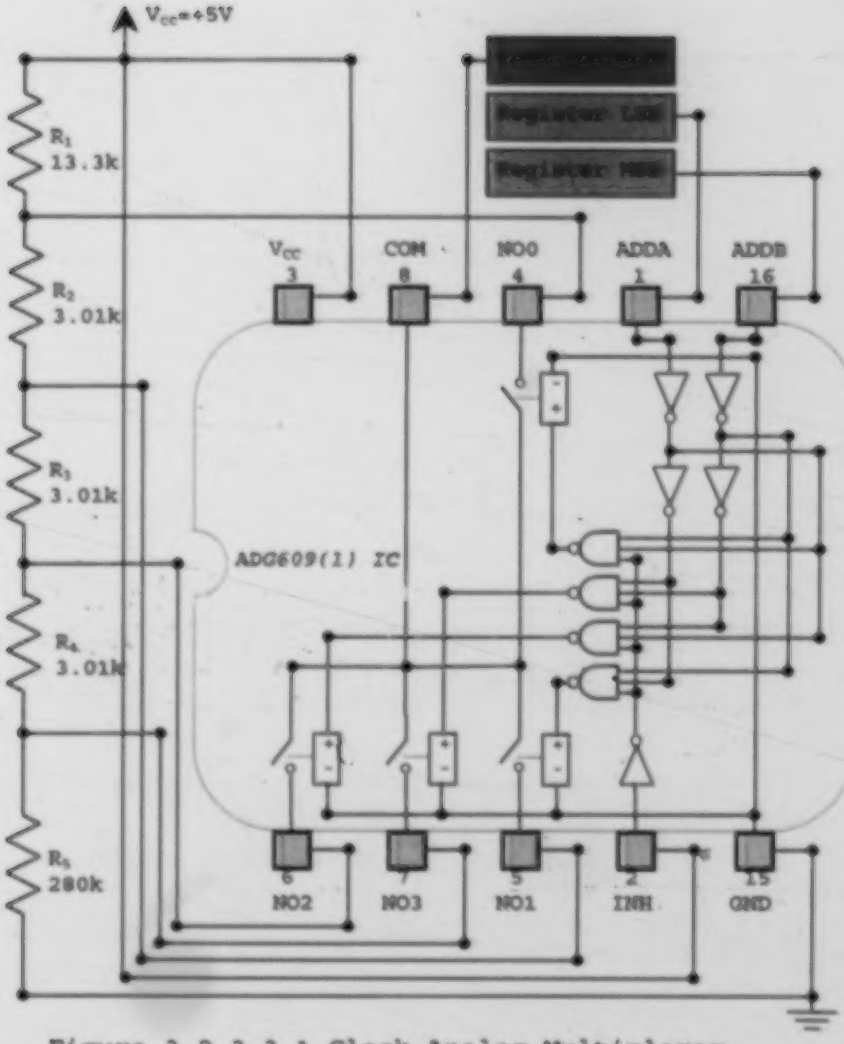


Figure 3.2.3.3.1 Clock Analog Multiplexer

3.2.4 Counter Circuit

3.2.4.1 Counter Introduction

The counter is a self-contained integrated circuit package. The counter circuit sequentially generates and facilitates the selection of new sensor addresses. The binary output of the counter determines which photodiode sensor is sampled as the new value at the negative comparator terminal. The clock drives the counter and the counter drives the counter analog multiplexer. The counter changes its output state when triggered by a negative clock pulse edge. The counter assumes a value between zero (0b00) and three (0b11). Each counter output state represents the address of a particular input/sensor channel. Counter output characteristics include a 40ms, $+5V_{DC}$ logic "1", or a 40ms, $0V_{DC}$ logic "0" pulse present on a two wire parallel address bus.

3.2.4.2 Counter Design

Integrated circuit counters are available from many manufacturers with many features. All counter integrated circuits have a minimum of four output bits. Four output bits is something of an over design; it is exactly twice as much circuitry as is required for this application.

Minimizing circuit area and still providing the essential functionality requires the exploration of options. It is important to note that much time was spent developing a dual function device from a quad flip-flop integrated circuit. Flip-flops are the building blocks of both counters and registers. It was hoped that the single integrated circuit could be connected to perform the dual functions of counter and register.

Two flip-flops can be connected to function as a two-bit counter. Two more flip-flops can be connected to function as a two-bit register. The hope was that with the right quad flip-flop integrated circuit, circuit area could be consolidated. An individual counter integrated circuit and an individual register integrated circuit would require at least twice as much circuit area as a single, dual function, integrated circuit.

A limited number of quad flip-flop integrated circuits are commercially available. In terms designing a counter, virtually any of these packages can be used. Trouble arises with the design of a register. To set a register value, the number of inputs must equal the number of bits in the register. Available quad flip-flop packages do not support the parallel setting of flip-flop values. In addition to this limitation, if the counter is a negative

edge triggered subsystem, then the controller design is more stable if the register is a positive edge triggered subsystem, or visa versa. This is because the inputs at the comparator must have a finite amount of time to set and become stable prior to making a comparison. The setting of the comparator inputs takes place on one clock transition. The effect of the comparison takes place on the inverse transition. There are no quad flip-flop packages available with more than one clock input or with both positive and negative transition flip-flops. The time spent developing a dual function device from a quad flip-flop integrated circuit ended without realization of the hope. However, the effort did lend itself to a deeper understanding of the logic components and operation of the counter and register circuits.

The National Semiconductor MM54C93 integrated circuit is a negative-edge triggered, count-up counter. The MM54C93 is available in a 14 pin, 8mm by 19mm molded dual inline package. The package operates with a single supply voltage (V_{CC}) between $+3V_{DC}$ and $+15V_{DC}$. The package dissipates between 500mW and 700mW and operates between -55°C and +125°C. The design is connected to use the $+5V_{DC}$ voltage supply. Use of this particular counter is

suggested in the prosthetic controller design as it has best essential features for the design.

The binary output of the counter determines which photodiode sensor is sampled as the new value. Counter output addresses and sensor addresses are mapped one to one. During the sample time the counter analog multiplexer closes a switch and enables the comparison of the analog value of the counter (new) photodiode sensor at the negative terminal of the comparator. A negative transition on the next clock pulse causes the counter to make its transition to the next state. During this time the next sensor channel is sampled and compared. The design is implemented as a count up counter. The next counter state is the previous value of the counter plus one. After a maximum of three state changes, the counter will reach its maximum binary value of 0b11. Upon the next transition, the counter takes the binary value 0b00. It is of interest to have the address values cycle in this way. The cycling feature enables the circuit to sample each sensor, one after another, ad infinium.

While synchronizing the operation of all flip-flops with a single clock is a common practice, the prosthetic controller benefits by interlacing the triggering for the counter and register. Interlaced triggering allows two

operations to take place in the span of a single clock cycle. The comparison of the analog output voltage of the counter (new) photodiode sensor with the analog output voltage of the register (registered) photodiode sensor begins during the negative clock transition. While the clock is at logic "0", the comparator sets the register mode to either synchronous parallel load mode or clock inhibit mode. When the comparator output is logic "0", the register enters the clock inhibit mode. When the comparator output is logic "1", the register enters the synchronous parallel load mode. The counter output is connected to the register input. The clock makes a positive transition from logic "0" to logic "1". If the register is in the synchronous parallel load mode, the new photodiode sensor address of the counter is loaded into the register while the clock is in the logic "1" portion of its cycle. If the register is in clock inhibit mode just prior to the positive clock transition, then the clock transition will fail to allow the updating of the register with the new photodiode sensor address.

An MM54C93 integrated circuit provides the new input address selection function for the prosthetic controller design. The MM54C93 counter uses clocked J-K flip-flops to hold the value of each of two the output address bits. By

constructing a two bit cyclic counter using only clocked J-K flip-flops and reviewing the logic diagram of the MM54C93 counter circuit, a MM54C93 integrated circuit is implemented within the prosthetic controller as a two bit counter.

The J-K input requirements of the counter are summarized within Table 3.2.4.2.1. The Q parameter refers the flip-flop output value for given values of J and K. The Q^* parameter represents the next value Q takes for the given input, J and K, and output Q.

Table 3.2.4.2.1: J-K Flip-Flop Input

J	K	Q	Q^*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

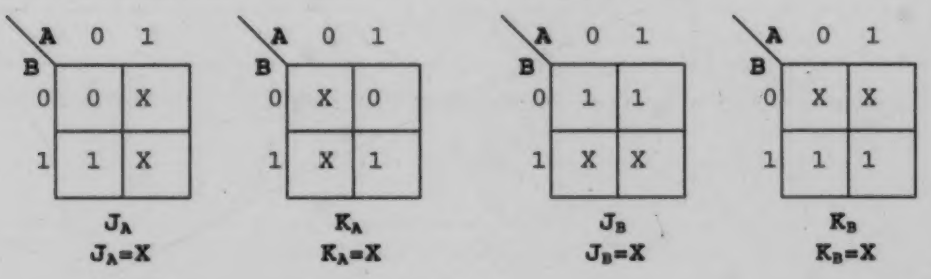
The first step in the design of a two bit J-K flip-flop counter is the construction of a state table (Table 3.2.4.2.2) from the known J-K flip-flop input table. Parameters A and B are the output values (Q_A and Q_B) of flip-flops A and B respectively. Parameters A^+ and B^+ are next state output values for Q_A and Q_B flip-flops A and B respectively. The X value refers to a parameter whose value does not affect the next A^+ or B^+ value. Parameters J_A and K_A are the input conditions, J and K, for flip-flop A. Parameters J_B and K_B are the input conditions, J and K, for flip-flop B. The counter state table representation in 3.2.4.2.2 has four possible states (four possible combinations of A and B output). Each state has a single next state associated with it (combinations of A^+ and B^+).

Table 3.2.4.2.2: State Table

A	B	A^+	B^+	J_A	K_A	J_B	K_B
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

The state table can then be re-represented with Karnaugh maps, as seen in Table 3.2.4.2.3. Karnaugh maps better enable the derivation of the input equations, and logic diagram; these will describe the desired behaviors for flip-flops A and B.

Table 3.2.4.2.3: Karnaugh Maps



From the Karnaugh maps, a logic diagram can be constructed. The Karnaugh maps allow a great amount of liberty in determining the flip-flop input equations; in fact, the solutions for the parameters J_A, K_A, J_B, and K_B can be set to "X". This means that each flip-flop changes state independent of output parameters Q_A and Q_B. The clock alone can trigger the state transitions for each flip-flop.

When the input equation of flip-flop A depends on flip-flop B output, or visa-versa, one clock may be used to synchronize both flip-flops. By setting the parameters J_A, K_A, J_B, and K_B to "X", one of two counter solutions must be employed to synchronize state changes for each flip-flop.

The first counter solution is to have two clocks. The second clock must operate at twice the frequency of the first clock. The second clock supplies the clock input to the flip-flop representing the Least Significant Bit (LSB) of the counter, and the first clock supplies the clock input to the flip-flop representing the Most Significant Bit (MSB) of the counter. Both clocks should operate in phase with each other. In phase with each other means that for the first clock, its transitions should take place when the transitions of the second clock take place.

The prosthetic design uses the second counter solution. This approach is referred to as the ripple clock. The ripple clock approach requires a single clock and a simple timing dependency between the LSB flip-flop and the MSB flip-flop. The clock need only be a pulse train with a non-periodic frequency. The ripple clock allows both synchronous and asynchronous operation of the counter. The prosthetic control design happens to require a synchronous clock. The ripple clock operates synchronously when the clock input is periodic and only a few flip-flops are used. Multiple flip-flops will result in a lag between the setting of the LSB and the MSB. Two flip-flops (two bits) connected as a counter in a ripple clock manner will generate an LSB and MSB in near

synchronicity relative to the overall length of the clock period.

The output of the clock circuit is the clock input for flip-flop B. The output of flip-flop B is the counter LSB. The output is a square wave with a 50% duty cycle alternating between $0V_{DC}$ and $+5V_{DC}$. The output has half the frequency of the clock output. The half frequency arises because the flip-flop only changes state on a negative edge trigger. Two negative edges of the clock (two periods) are required to flip one bit within the flip-flop. The output from flip-flop B is connected to the clock input of flip-flop A. The output of flip-flop A is a square wave with a 50% duty cycle alternating between $0V_{DC}$ and $+5V_{DC}$. The output has half the frequency of flip-flop B. This output is the MSB of the counter.

Figure 3.2.4.2.4 is the logic diagram constructed from the Karnaugh Map. The logic diagram contains the circuit elements and the connection of those circuit elements necessary to construct a two bit counter circuit. If the logic diagram of Figure 3.2.4.2.4 is compared to the logic diagram of the MM54C93 counter circuit in Figure 3.2.4.2.5, the realization of a two bit counter from the MM54C93 circuit may be completed. Figure 3.2.4.2.5 illustrates the MM54C93 circuit connected to realize a two bit counter.

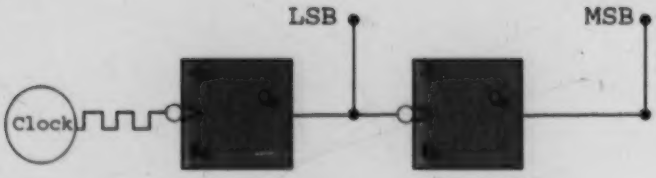


Figure 3.2.4.2.4 Counter Logic Diagram

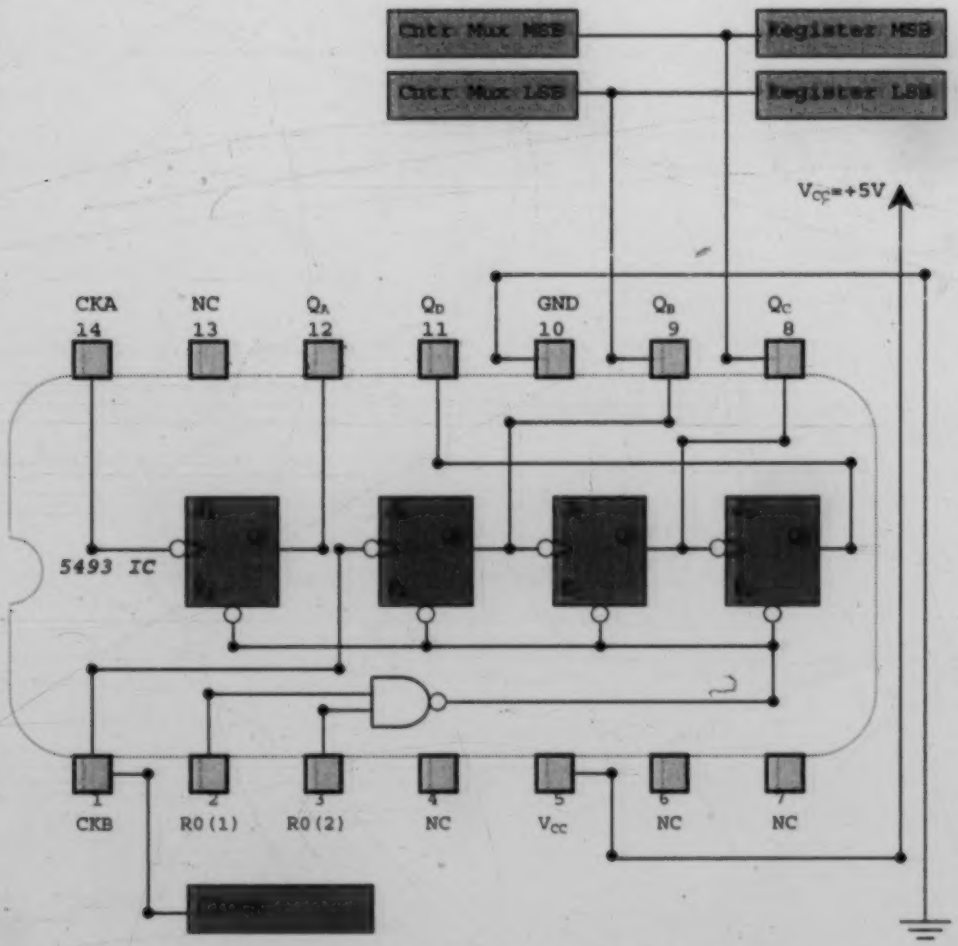


Figure 3.2.4.2.5 Counter Circuit Diagram

3.2.5 Counter Analog Multiplexer Circuit

3.2.5.1 Counter Analog Multiplexer Introduction

The counter analog multiplexer is a self-contained integrated circuit. The function of the counter analog multiplexer is to close one of four switches between four analog inputs and a common output. The output of the counter analog multiplexer is the voltage seen across one of four photodiode sensors. The counter output is connected to the digital input of the counter analog multiplexer. A new counter output state sets the digital input of the counter analog multiplexer and causes the multiplexer to switch to a new state. Each unique counter analog multiplexer digital input state results in an output of the associated sensor's analog voltage at the common output. Each multiplexer switch closes, one after another, ad-infinium. The closed switch connects the associated analog sensor input channel to the negative terminal of the comparator circuit.

3.2.5.2 Counter Analog Multiplexer Design

The counter analog multiplexer is designed with the MAX4524 analog multiplexer integrated circuit. Ideal for this prosthetic design, the package is a four channel

analog multiplexer with a common output. The MAX4524 package operates with a single supply voltage ranging between $+2V_{DC}$ and $+12V_{DC}$. It is available in a ten pin, 3mm x 5mm μmax package, with a power dissipation of 330mW below +70°C. The prosthetic design is connected with a $+5V_{DC}$ voltage supply. The resistance across a closed switch is 200Ω when a single $+5V_{DC}$ voltage supply is employed.

The counter analog multiplexer switches exactly one of four separate analog inputs to a common output depending on the output address of the counter and an enabling input. The enabling input of the counter analog multiplexer is grounded. Grounding the enabling input enables the counter analog multiplexer at all times. The integrated MAX4524 decoder actuates four switches. Each voltage-controlled switch has one of two positions. Switches integrated onto the analog multiplexer can remain either opened or closed. The MAX4524 analog multiplexer switches normally remain open, except for one switch referenced by the decoder. Corresponding to the digital input address, the integrated decoder closes a single voltage-controlled switch and opens the other three switches. Table 3.2.5.2.1 illustrates this logic in a tabular form. The closed switch is shorted to the common output across a 200Ω internal resistance. The

200Ω internal resistance of the counter analog multiplexer is small relative to the input resistance of the photodiode resistive network. More importantly, the 200Ω internal resistance is very small relative to the input resistance of the comparator circuit. This means that the 200Ω resistance does not sizably affect the photodiode signal level seen at the comparator input. The voltage seen at the common analog output is, arguably, the photodiode voltage.

Table 3.2.5.2.1: Counter Analog Multiplexer Truth Table

INH	ADDA	ADDB	ON Switch
1	X	X	NONE
0	0	0	COM-NO0
0	0	1	COM-NO1
0	1	0	COM-NO2
0	1	1	COM-NO3

The counter analog multiplexer cycles the closing of each switch in response to new counter states. Digital output from the counter is connected to the digital input

of the counter analog multiplexer. The counter analog multiplexer changes state every 20ms in synchronicity with changes in counter output. Multiplexer switches close for 20ms each, one after another, ad-infinium. This cycling allows all four sensor input channels to be sampled, one after another for 20ms each, over a period of 80ms.

Figure 3.2.5.2.2 illustrates the complete counter analog multiplexer, its digital and analog inputs and its common output. The digital address output of the counter is connected directly to the digital inputs of the counter analog multiplexer. The least significant bit of the counter is connected to the ADDA terminal of the multiplexer. The most significant bit of the counter is connected to the ADDB terminal of the multiplexer. The digital enable (INH) input of the counter analog multiplexer is permanently connected to the ground reference. Each analog input (NO0 through NO3) of the analog multiplexer is connected to a photodiode sensor and its input resistive network. The negative terminals of the switches are connected to a common output (COM). Only one switch is ever closed at any time for a given decoder. The common analog output (COM) is connected to the negative input terminal of the comparator circuit.

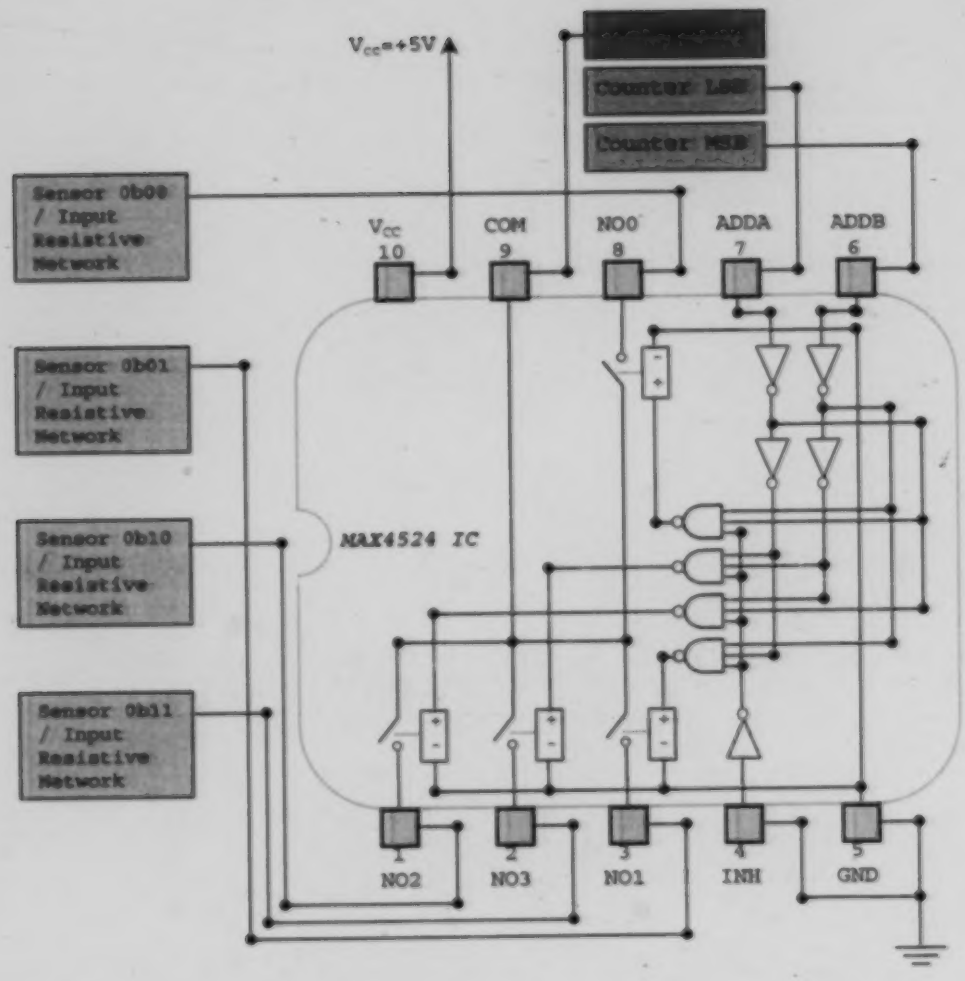


Figure 3.2.5.2.2 Counter Analog Multiplexer Circuit

3.2.6 Register Circuit

3.2.6.1 Register Introduction

The register is a self-contained integrated circuit package. Storing and facilitating the selection of the address of a photodiode sensor absorbing the least light at any given moment is the function of the register. A voltage level present at the register photodiode sensor is the real-time analog reference (register) value compared within the prosthetic controller at the positive terminal of the comparator circuit. The counter, comparator and clock circuits drive the register. Register output lends in updating the position of the actuator. The two bit digital output of the register is the digital input to both the register analog multiplexer and the clock analog multiplexer. The clock analog multiplexer and register analog multiplexer happen to be the same dual function integrated circuit. The register assumes a binary output value between zero (0b00) and three (0b11). Each binary output state represents the address of particular input/sensor channel. Register output characteristics include a 20ms pulse. Either a $+5V_{DC}$ logic "1" or $0V_{DC}$ logic "0" is present on a two wire parallel address bus.

3.2.6.2 Register Design

Integrated circuit registers are available with several different options. Shift left, shift right, clear, parallel input, serial input, latched inputs and multiplexed serial input functions are available. Integrated circuit registers are available from many manufacturers; all of these registers have a minimum of four input/output bits. Four input/output bits is an over design for this application; it is exactly twice as much circuitry as is required. As stated in section 3.2.4.2, a limited number of quad flip-flop integrated circuits are commercially available. To set a register value, the number of binary inputs must be equal to the number of bits in the register. Available quad flip-flop packages do not support the parallel setting of register values. In addition to this limitation, the counter is negative-edge triggered and the register is positive edge-triggered subsystem. There are no quad flip-flop packages available with more than one clock input and/or both negative and positive edge-triggered flip-flops. It is for these reasons that an integrated circuit register having four input/output bits is the only choice at this time.

The Texas Instruments SN54AS194 4-bit bi-directional universal shift register integrated circuit comes in a

fourteen pin, small outline and 300-mil dual inline package. Register flip-flops are positive edge-triggered. Dissipating 200mW of heat, the package operates at temperatures between -55°C and +125°C, with a single +5V_{DC} voltage supply. This counter has the best essential features for the prosthetic controller design.

The value of the register determines which photodiode sensor address is sampled as the reference (register) value and indirectly facilitates the setting of the actuator position. Identical to the counter, register values and sensor addresses are mapped one to one. During the sample time the register analog multiplexer closes a switch and enables the comparison of the analog value of the reference sensor channel at the positive terminal of the comparator. Opposite to the counter, a positive edge on the clock pulse causes the register to make its transition to the next state.

A counter (new) photodiode sensor absorbing less light than the reference photodiode sensor, when sampled, causes the comparator to take a logic "1" output state. Comparator output of logic "1" connected to the register mode terminals, cause the register to enter the synchronous parallel load mode. The counter output is connected to the register parallel load input. When the register is in the

synchronous parallel load mode and triggered by a positive clock transition, the register takes the photodiode address value of the counter; the new reference photodiode sensor address is the new photodiode sensor address of the counter.

A new photodiode sensor absorbing more light than the reference photodiode sensor, when sampled, causes the comparator to take a logic "0" state. A comparator output of logic "0" connected to the register mode switches, causes the register to enter a clock inhibit, do nothing mode. Upon a positive going clock transition, the register retains the previously loaded reference photodiode sensor address; this mode inhibits the clock from altering the state of the register.

Table 3.2.6.2.1 and Figure 3.2.6.2.2 succinctly describe the logic of the register. Two modes of register operation, synchronous parallel load mode and clock inhibit mode, allow the register to update and retain the address of the photodiode sensor absorbing the least light at any given moment in time. The register photodiode address value is retained for a minimum of 20ms. During this time the register address output indirectly stimulates the position update of the prosthetic actuator. Figure 3.2.6.2.3 illustrates the connection of the 5493 circuit.

Table 3.2.6.2.1 Register Truth Table

Function Table											
INPUTS								OUTPUTS			
	MODE			PARRELLEL							
-CLR	S1	S0	CLOCK	A	B	C	D	Q_A	Q_B	Q_C	Q_D
0	X	X	X	X	X	X	X	0	0	0	0
1	X	X	0	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
1	1	1	↑	a	b	c	d	A	B	C	D
1	0	0	↑	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

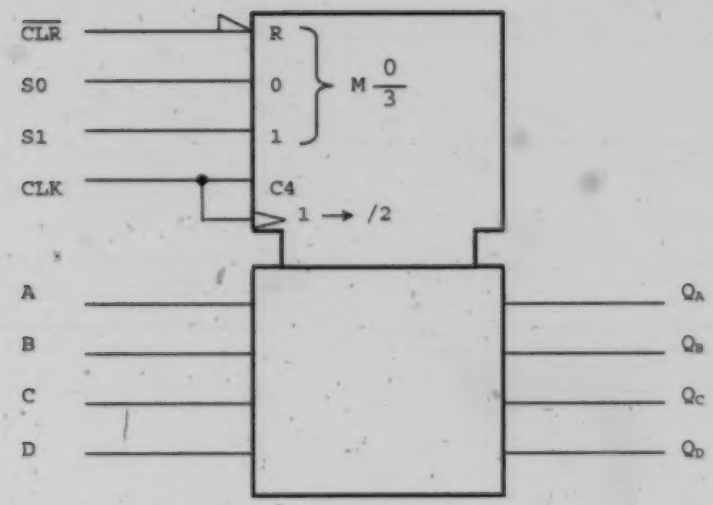


Figure 3.2.6.2.2 Register Logic Symbol

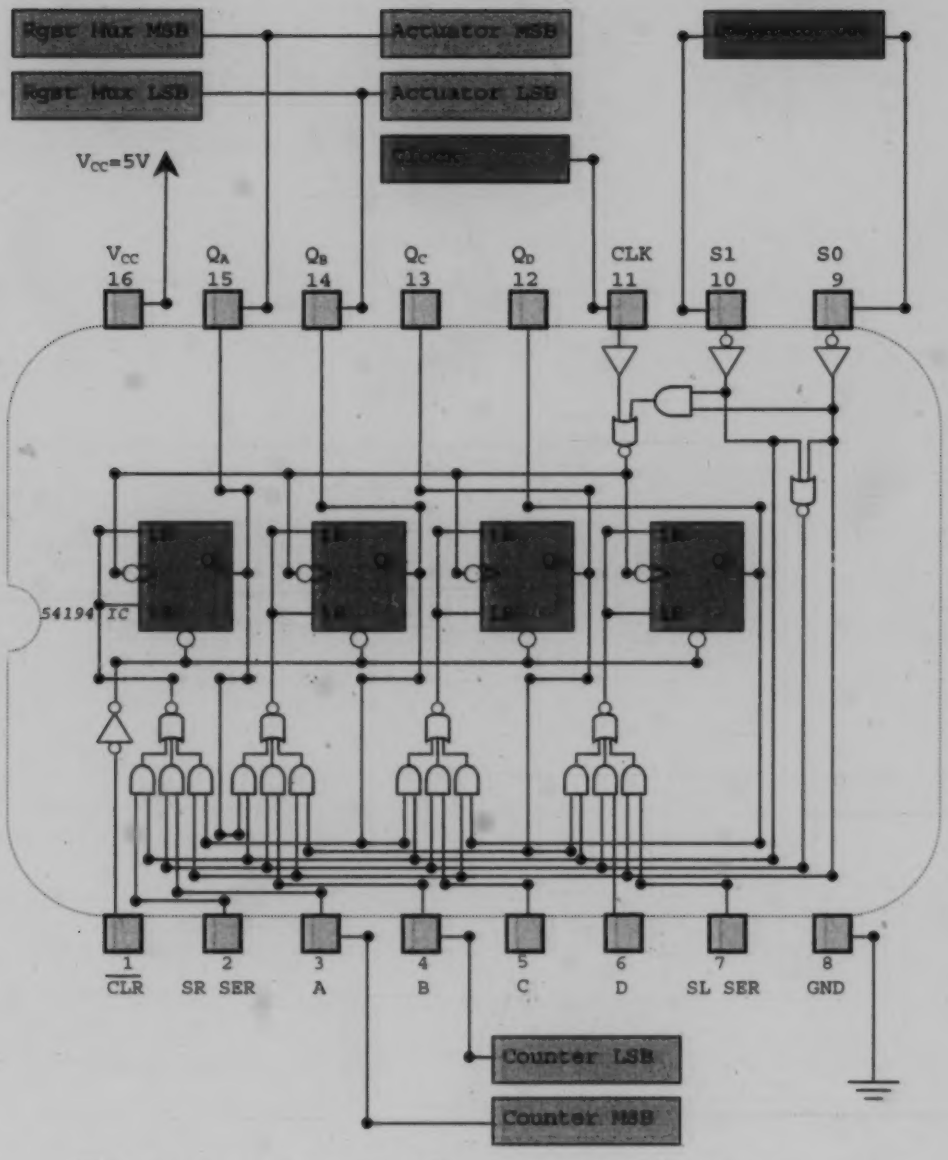


Figure 3.2.6.2.3 Register Circuit Diagram

3.2.7 Register Analog Multiplexer Circuit

3.2.7.1 Register Analog Multiplexer Introduction

Like the counter analog register, the register analog multiplexer is a self-contained integrated circuit. The function of the register analog multiplexer is to close one of four switches between four analog inputs and a common output. The output of the register analog multiplexer is the voltage seen across one of four photodiode sensors. The register output is connected to the digital input of the register analog multiplexer. When the register takes a new output value, this value sets the shared digital input of the register analog multiplexer and the clock analog multiplexer. This causes the multiplexers to change state. In reference to only the register analog multiplexer, the switch associated with the multiplexer digital input closes. The closed switch connects the associated sensor input channel to the positive input terminal of the comparator circuit.

3.2.7.2 Register Analog Multiplexer Design

The ADG609 package is a dual four channel analog multiplexer with two common outputs. The ADG609 differential, dual 4 channel, low voltage analog

multiplexer is shared between the clock circuit and the register circuit. The package operates at $+3V_{DC}$ or $+5V_{DC}$ and is available in a 16 pin, 6mm x 10mm SOIC package, with a power dissipation of 1.50µW below +70°C. The prosthetic design is connected with a $+5V_{DC}$ voltage supply. The resistance across a closed switch is 30Ω when a single $+5V_{DC}$ voltage supply is employed.

The register analog multiplexer switches exactly one of four analog inputs to a common output depending on the output address of the register and an enabling input. Unlike the counter analog multiplexer, the enabling input of the register analog multiplexer is permanently connected to the $+5V_{DC}$ voltage supply. Permanently retaining the enable pin of the register analog multiplexer at the $+5V_{DC}$ voltage reference keeps this multiplexer enabled at all times. The ADG609 decoder actuates four switches. Each voltage-controlled switch has one of two positions. Switches integrated onto the analog multiplexer can remain either opened or closed. The ADG609 analog multiplexer switches normally remain open, except for one switch referenced by the integrated decoder. Corresponding to the digital input address, the integrated decoder closes a single voltage-controlled switch and opens the other three switches. Table 3.2.7.2.1 illustrates this logic in a

tabular form. The closed switch is shorted from an input to the common output across a 30Ω internal resistance. The 30Ω internal resistance of the counter analog multiplexer is small relative to the input resistance of the photodiode resistive network. More importantly, the 30Ω internal resistance is very small relative to the input resistance of the comparator circuit. The 30Ω resistance does not sizably affect the photodiode signal level seen at the comparator input. The voltage seen at the common analog output is, arguably, the photodiode voltage. The fact that the register analog multiplexer resistance is not perfectly matched to the counter analog multiplexer resistance is of little consequence because of the large input impedance values. A 170Ω resistance can also be placed between the multiplexer common output and the comparator input.

Table 3.2.7.2.1: Register Analog Multiplexer Truth Table

EN	ADDA	ADDB	ON Switch
0	X	X	NONE
1	0	0	COM-NO0
1	0	1	COM-NO1
1	1	0	COM-NO2
1	1	1	COM-NO3

The register analog multiplexer closes the associated switch in response to new register states. Digital output from the register is connected to the digital input of the register analog multiplexer. The register analog multiplexer can change state every 20ms in synchronicity with changes in register output. Real-time comparatively, the register value changes each time a new photodiode sensor, receives less light than the previously registered photodiode sensor channel. The register analog multiplexer may never change state if the registered photodiode sensor channel is continuously receiving less light than the other photodiodes.

Figure 3.2.7.2.1 illustrates the complete register analog multiplexer, its digital and analog inputs and its common output. The output of the register is connected directly to the digital inputs of the register analog multiplexer. The least significant bit of the register is connected to the ADDA terminal of the multiplexer. The most significant bit of the register is connected to the ADDB terminal of the multiplexer. The digital inputs (ADDA and ADDB) serve as switch address references. The digital enable (INH) input of the register analog multiplexer is permanently connected to the $+5V_{DC}$ voltage source. Each

analog input (NO0 through NO3) of the analog multiplexer is connected to a photodiode sensor and the input resistive network. The negative terminals of the switches are connected to a common output (COM). This common output does not affect the isolation of the input resistive networks. Only one switch is ever closed at any time for a given decoder. The common analog output (COM) is connected to the positive terminal of the comparator circuit.

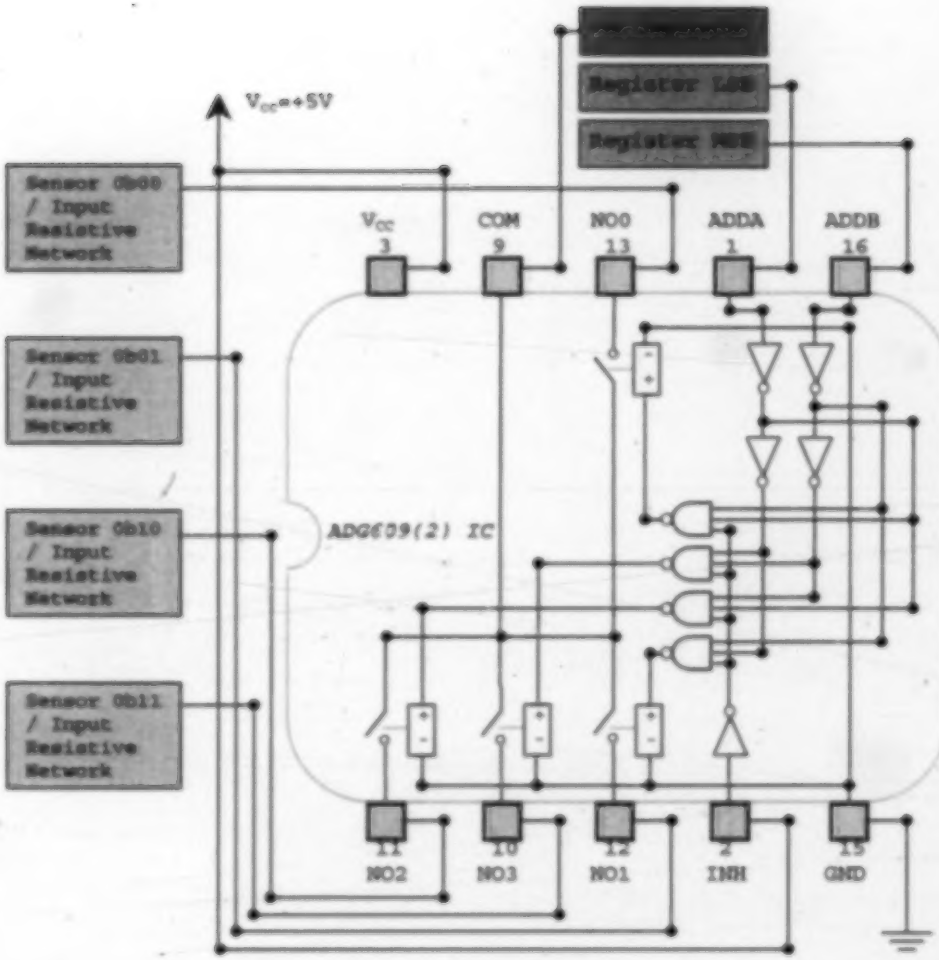


Figure 3.2.7.2.2 Register Analog Multiplexer Circuit

3.2.8 Comparator Circuit

3.2.8.1 Comparator Introduction

The comparator circuit is a self-contained integrated circuit package. Present at the comparator inputs, the analog voltage value of the counter photodiode sensor resistor is compared with the analog voltage value of the register photodiode sensor resistor. Comparator output is $0V_{DC}$ logic "0" when the register photodiode sensor absorbs less reflected light than the counter photodiode sensor. Conversely, the comparator output is $+5V_{DC}$ logic "1" when the register photodiode sensor absorbs more reflected light than the counter photodiode sensor. This digital comparator output signal is present on a single output wire connected to the register mode terminals S0 and S1. The comparator output determines if the counter (new) photodiode sensor address value is uploaded to the register. In brief, when the comparator output is logic "1", the register enters the synchronous parallel load mode, on a positive clock transition, the counter uploads its output address to the register. When the comparator output is logic "0", the register enters the clock inhibit mode and the register retains its present value. Details of the operation of the comparator circuit follow.

3.2.8.2 Comparator Design

After simulating the operation of several comparator integrated circuit products within the prosthetic controller, the Maxim MAX975ESA comparator proved to have the most stable and desirable characteristics for use within the prosthetic controller application. A comparator is a special class of operational amplifier, where the device is used to compare signal voltages between the two inputs. The Maxim MAX975ESA integrated circuit is optimized for $+3V_{DC}$ or $+5V_{DC}$ single supply, rail to rail, infrared receiver applications. Consistent with the voltage supply employed, the prosthetic design is connected with a $+5V_{DC}$ voltage supply. The MAX975 comparator is available in a 3mm by 5mm, 8 pin, small outline package. The comparator operates between -40°C and +85°C, and dissipates 330mW of power. Both the comparator Power Supply Rejection Ratio (PSRR) and the Common Mode Rejection Ratio (CMRR) take a typical value of 90dB. High values of PSRR and CMRR lend to a high degree of noise immunity. PSRR and CMRR are essentially the same value. The real difference lies in the fact that the CMRR affects only the differential amplifier, whereas the PSRR affects the output stage too. Effects due to both CMRR and PSRR can be represented as small voltage generators inserted in series

with one of the comparator leads. Three comparator modes of operation are available. The comparator can operate in a high-speed mode, a low power mode, and a stand-by mode.

The high-speed comparator mode sinks 300μA of source current and results in a 28ns propagation delay. The low power mode of operation the supply current drops to 5μA and the propagation delay increases to 480ns. In the auto-standby mode, the comparator switches into low-power standby for a comparator with unchanged inputs. Although for this application, the low-power and auto-standby modes are not implemented, the auto-standby timeout period is easily adjustable by means selecting and inserting an external capacitor.

Like most every other comparator, the Maxim MAX975 has a negative input terminal, a positive input terminal, and a single digital output. The MAX975 comparator circuit provides an indication of the relative state of the potentials at its input terminals. The positive input comparator terminal serves as a reference potential. This reference potential is the voltage seen across the input resistive network of the sensor multiplexed through the register analog multiplexer (register). The negative input comparator terminal serves as a testing potential. This testing potential is the voltage seen across the input

resistive network of the sensor multiplexed through the counter analog multiplexer (new). The comparator output indicates whether the testing potential is greater than the reference potential. Comparator output is $0V_{DC}$ logic "0" when the reference potential is less than the testing potential. Comparator output is $+5V_{DC}$ logic "1", when the testing potential is less than the reference potential.

For the sake of thoroughness, it is important to discuss the comparator hysteresis characteristics. When the comparator inputs have the same analog values, the output takes on an indiscriminate state of $+2.5V_{DC}$. The comparator output can only take on an indiscriminant state should both input levels be identical for a considerable time period. This indiscriminant state would be something of a rarity. Section 4.2 demonstrates that even slowly converging inputs do not readily generate an indiscriminant output. The MAX975 comparator has an internal hysteresis to counter parasitic effects and noise. Hysteresis in the comparator creates two trip points: one for the rising input and one for the falling input. The difference between the trip points is the hysteresis. When comparator input voltages are equal, the hysteresis effectively causes one comparator input to move quickly past the other, taking the input out of the region where oscillations can occur.

The comparator output value is updated in real-time, based upon the positive and negative inputs. There is no minimum duration for which the digital output value stands; Comparator output is updated as quickly as the input references change. Only a propagation delay of 28ns is required to update the digital output of the comparator. This digital signal manifests on a single comparator output lead connected directly to the register mode terminals S0 and S1. As stated, the comparator output determines if the counter (new) photodiode sensor address value is uploaded to the register. When the comparator output is logic "1", register input S0 and S1 are logic "1" and the register enters the synchronous parallel load mode. When the comparator output is logic "0", register input S0 and S1 are logic "0", and the register enters the clock inhibit mode. Figure 3.2.8.2.1 illustrates the comparator circuit connection and operation within the prosthetic controller.

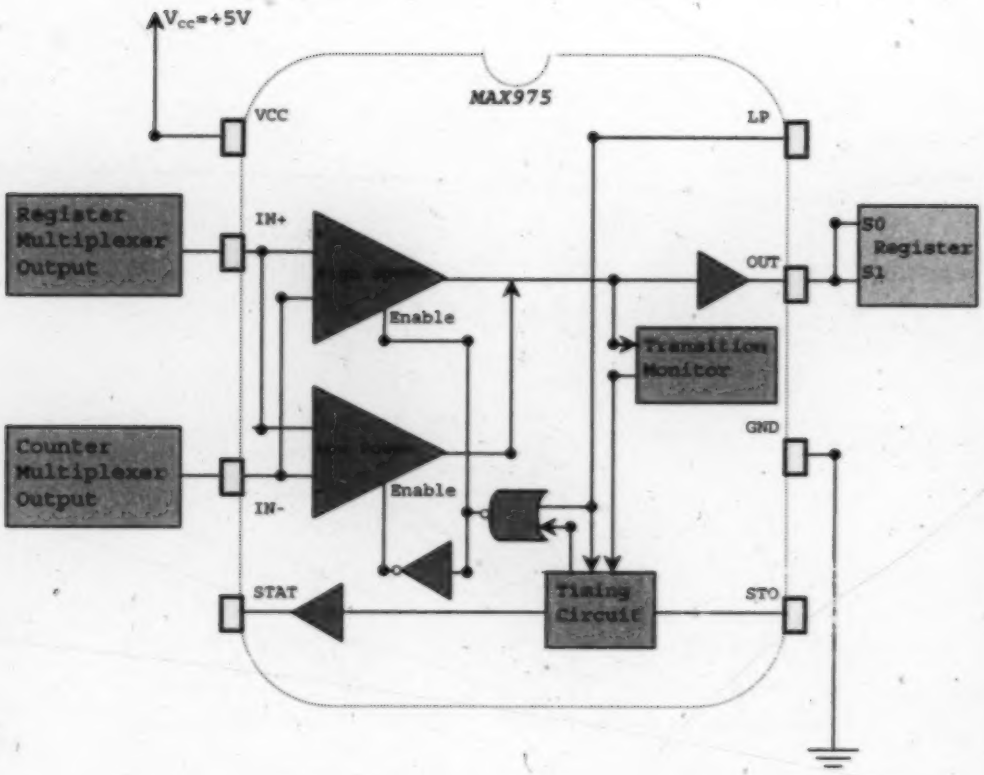


Figure 3.2.8.2.1 Comparator Circuit Diagram

3.2.9 Prosthetic Eye Actuator

3.2.9.1 Actuator Introduction

References to the input signal characteristics for servomotors and servomotor amplifier electronics are obscure. Rather than spending valuable time searching for information that may not exist, an alternate design approach is taken for this portion of the controller. It should not go without saying that much time was spent searching for literature. Reviewed literature refers to a "3-wire unmodified servo" and specifies some of the characteristics of a servo and the servo electronics without referring to any one specific servo [Jones et al. 1993]. Design of the prosthesis is based upon referenced characteristics of a 3-wire unmodified DC servomotor capable of processing pulse-width coded position signals. The servomotor is connected as a closed-loop position control system. The integrated servo amplifier decodes pulse-width coded position signals encoded within the clock output. Four unique pulse-width signals are sent to the servo amplifier. A decoded signal allows the single axis servomotor to turn in either direction. The servomotor is connected via a gear assembly to a miniature linear actuator. The actuator assumes a steady state at one of

four positions along the length of the actuator as portrayed in Figure 3.2.9.1.1.a and 3.2.9.1.1.b. The linear actuator is connected to the posterior face of the prosthetic eye via elastic threads and rotates the prosthesis about a post.

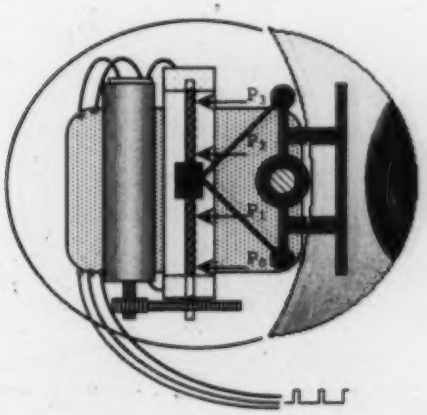


Figure 3.2.9.1.1.a Top View Prosthetic Eye

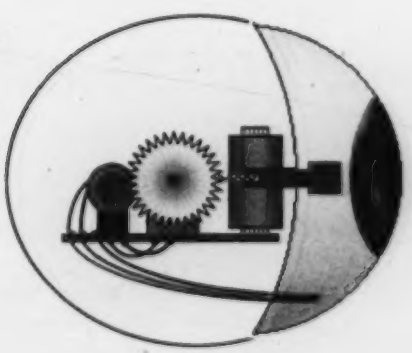


Figure 3.2.9.1.1.b Side View Prosthetic Eye

3.2.9.2 Actuator Design

The largest challenge in the selection of a suitable prosthetic eye actuator happens to be choosing a small enough actuator. The optical chamber is approximately 30mm deep and as wide and high. The German made WES Technik, Light Servo 3.5 is a 3.5g, 15mm by 20mm by 15mm, DC servo and linear actuator and fits within the optical cavity. The Light Servo 3.5 generates a maximum output force of 1.32N. It is capable of lifting a 135g weight when drawing 120mA of current. This output force surely exceeds the lateral weight and frictional forces of the prosthesis and the added resistive force of the eyelid against the prosthesis.

The servo operates at a nominal voltage of $+5V_{DC}$ with a maximum 120mA load current. Loaded, the actuator travels from end to end, a distance of 14mm, in 150ms, resulting in a time average speed of 93mm/s. The actuator cannot scan as quickly as the human eye during fast eye movements; however, during slow eye movements the actuator speed exceeds the speed of the human eye. When viewing the prosthesis relative to the human eye, the one speed, two direction, four position, actuator lags slightly during fast eye movements and "jerks" quickly from one position to another during slow eye movements.

Fortunately, the travel distance of the linear actuator between successive positions is limited to approximately 2.5mm, resulting in the prosthesis rotating by less than 15° per successive position change. This is demonstrated in Figures 3.2.9.2.1.a-d. The mechanics of the prosthesis movement can be tuned to allow a greater or lesser degree of rotation, other than the 45° full range of rotation specified, by adjusting the torque lengths of the pivot arms within the prosthesis.

The "3-wire unmodified servo" is connected to the $+5V_{DC}$ reference voltage, a ground, and the clock output. The clock output provides pulse-width coded position signals which the closed position control system decodes. Four unique pulse-width coded signals are sent to the servo amplifier electronics. These pulse-width signals (see Figures 3.2.3.2.1.a-d and Figures 3.2.9.2.1.a-d) activate the servomotor and the attached gear train. The two piece gear train is connected to a miniature linear actuator. The actuator takes one of four positions along the rail of the actuator. It is likely that some form of rotational position feedback is employed. This is verified in section 4.3. This position feedback should insure that the pulse width input characteristics achieve the desired position independent of the external load.

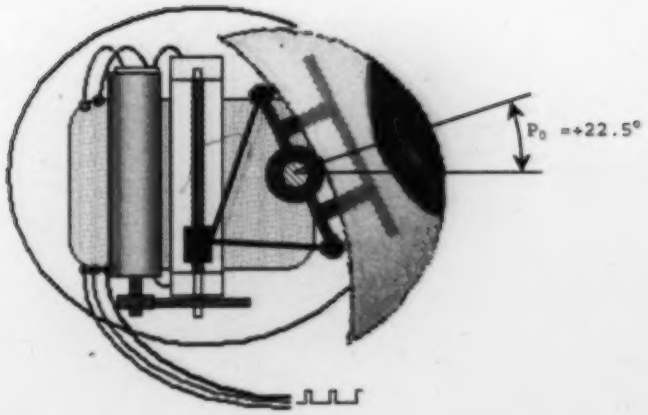


Figure 3.2.9.2.1.a Prosthetic Position 0b00

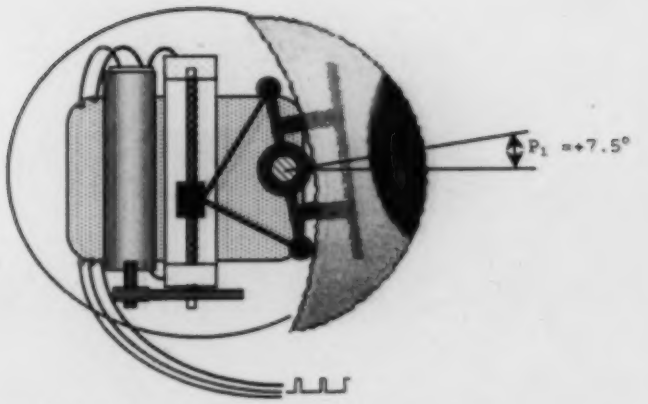


Figure 3.2.9.2.1.b Prosthetic Position 0b01

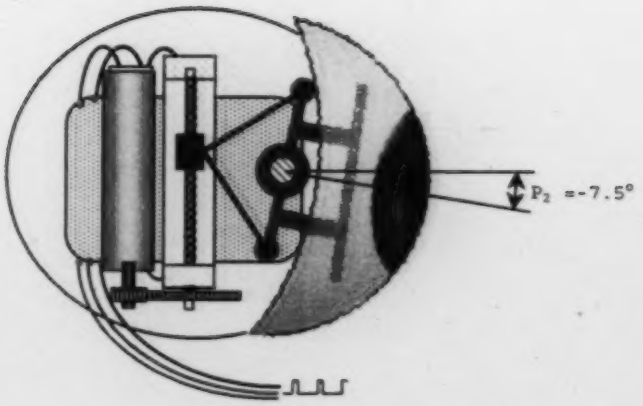


Figure 3.2.9.2.1.c Prosthetic Position 0b10

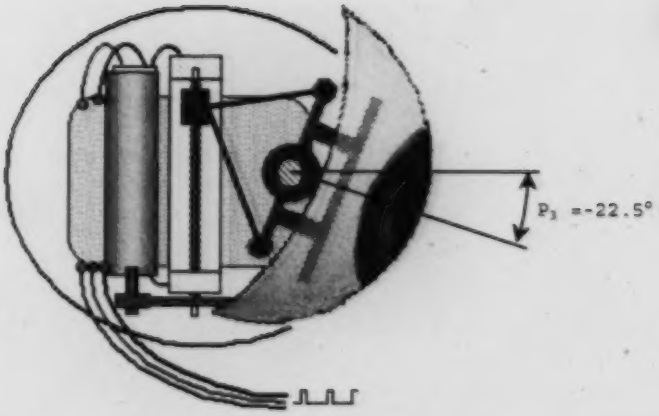


Figure 3.2.9.2.1.d Prosthetic Position 0b11

The option to connect the prosthesis to a power supply within the optical cavity and to optically transmit pulse-width data to the servo controller would eliminate the need to hide the external wire connections. Available optical prosthetics are limited by their lack of movement; however existing prosthetics do not have any external wires. The optical cavity is simply not large enough to accommodate both the servomotor and battery. Leads are a necessity.

Electric wire is manufactured as thin as 0.05mm in diameter. Wire this thin can easily be hidden, if only by overlooking it, but there are other considerations in the choice of wiring. A voltage stabilized power supply controls the voltage across its output terminals. Hence, the wire conductors used to connect the load must be considered as part of the load. At high load currents, the voltage drop across the supply leads may appreciably degrade stabilization of the load. Fortunately, very short lengths of wire are involved in this application. Wire impedance for low frequency signals for the smallest diameter wire is negligible in comparison to the servomotor load.

Current carrying capacity is defined as the amperage a conductor can carry before melting either the conductor or the insulation. Heat, caused by an electrical current

flowing through the conductor, will determine the amount of current a wire will handle. Theoretically, the amount of current that can be passed through a single bare conductor can be increased until the heat generated reaches the melting temperature of the conductor. There are many factors that limit the amount of current that can be passed through a wire. The most important of these considerations for this application is conductor size and ambient temperature. The larger the circular mil area, the greater the current capacity. The amount of heat generated should never exceed the maximum temperature rating of the insulation. The higher the ambient temperature, the less heat required to reach the maximum temperature rating of the insulation. Conductor and insulator size and composition is an important choice because a high tensile and bending strength for these unprotected wires is required. These considerations should be balanced with the value of achieving a thin wire cosmetically pleasing design. Taking into account the variables involved, a 30AWG wire is chosen for each of the three connecting wires.

A 30AWG solid copper wire has a diameter of 0.125mm and a circular area of 0.05mm^2, a DC resistance of 0.365Ω/m, and is rated between 2 and 4 amperes depending upon the

insulation. Irradiated polyvinychloride (PVC) nylon insulation allows 20AWG solid copper wire to carry three amperes of current at +105°C. The 120mA maximum servo load current easily fits into this wire choice. This choice of excessively large diameter wire allows the wire to withstand breaking when a 200g (2N) weight is applied.

4. Simulation and Experimental Results

In this chapter, results of the simulations and experiments that were performed on the prosthetic eye controller are presented. These results engender the design philosophy and ultimately shape the controller circuit from the highest level down to the most discrete choice of components. The controller data is represented in three environments: In the optical environment, input data, in the form of light, is obtained from infrared detectors. In the electrical environment, the transduced input data is conditioned and processed. Finally, in the mechanical environment, electrical information controls the rotation of the servomotor and ultimately sets the position of the actuator. Interactive Image Technologies, Electronics Workbench application is able to provide a suitable environment for the analysis of analog, digital and mixed circuits. However, some models, having optical or mechanical dependencies, cannot be fully simulated within this electrical environment. A photodiode detector is a light/electrical transducer. Voltage, current and impedance properties of the photodiode can be modeled. However, optical input parameters of the detector which

affect these electrical properties are completely outside of the range of this application's usefulness. Similarly, in the mechanical environment, simulation of the servomotor operation is limited to the electrical signals passed to the servo electronics for the same reasons already touched upon. Servomotor power, torque, speed, load and the relation of these properties to the electrical input must be obtained through experimentation. Section 4.1 embodies details of the photodiode sensor experiments. Section 4.2 discusses the simulation details of the controller tracking circuitry. Finally, details of the experiments performed on the servomotor are related in section 4.3.

4.1 Photodiode Sensor Experimentation

A transfer function that relates the input parameters of the photodiode detector to the output parameters of the detector cannot be achieved with the Electronics Workbench application. A solution to this problem is to perform real experiments on the infrared detectors. Sensors and there associated circuitry are assembled to gather empirical data in two experiments. The gathered information is used to model the output of the photodiode within the simulation environment, to tune the sensor resistive network and to optimize the physical/geometrical traits of the design.

The first photodiode experiment establishes the characteristics of the photodiode response to the ambient light level. Three photodiodes, as described in Figure 4.1.1, are connected to measure the photodiode response to light. A WAVETEK DM28XT digital multimeter measures the photodiode resistance values. The three photodiodes are placed side by side and each photodiode resistance is measured as a 40W light bulb is moved between 0.31m and 2.18m from the front face of the detectors. The exercise demonstrates how well matched the detectors are and the range of resistance values the detectors are expected to exhibit while being simulated and while connected to the prosthetic controller.

Figure 4.1.1 Simple Photodiode Test Circuit

The results of the first photodiode experiment are outlined in Table 4.1.2. During the testing an additional result was found somewhat by accident. It seems that a florescent tube light source contributes very little infrared light. This result may possibly limit the use of the prosthetic controller in a florescent light setting. The input resistive network is designed with a standard 1MΩ resistor value.

Table 4.1.2 Photodiode Output vs. Incident Radiant Light

d (m)	Intensity (W/m^2)	S1 (MΩ)	S2 (MΩ)	S3 (MΩ)
0.31	100	0.089	0.096	0.076
0.44	50	0.190	0.186	0.184
0.69	20	0.321	0.312	0.330
0.98	10	0.724	0.740	0.744
1.38	5	1.053	1.065	1.062
2.18	2	1.481	1.471	1.474

The final photodiode experiment plots the photodiode resistive network output voltage as a function of the photodiode position and distance from the pupil. Figure 4.1.3 illustrates the prototype photodiode test circuit and Figure 4.1.4 illustrates the output voltage as a function of the photodiode position and distance from the pupil. The X-axis is the relative rotation position of the pupil center with respect to the photodiode. The Y-axis is the normal distance of the photodiode from the surface of the

eyeball. The Z-axis is the voltage of the photodiode resistor for the X and Y parameters, when the photodiode is subject to $10W/m^2$ of ambient radiant intensity. The experiment demonstrates the need to keep the detector in close proximity to the eye to resolve the boundaries.

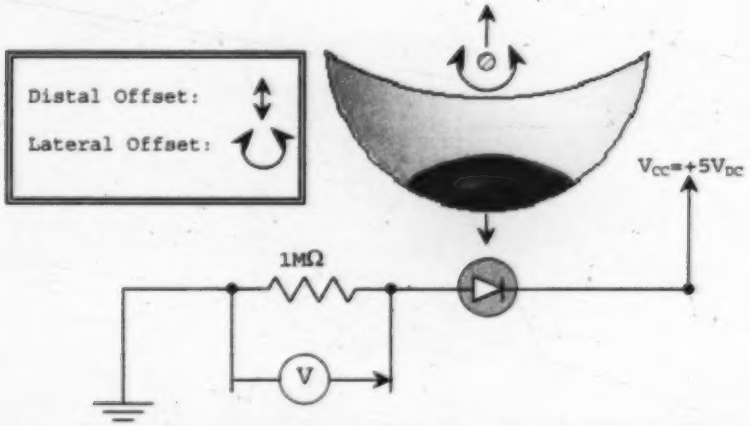
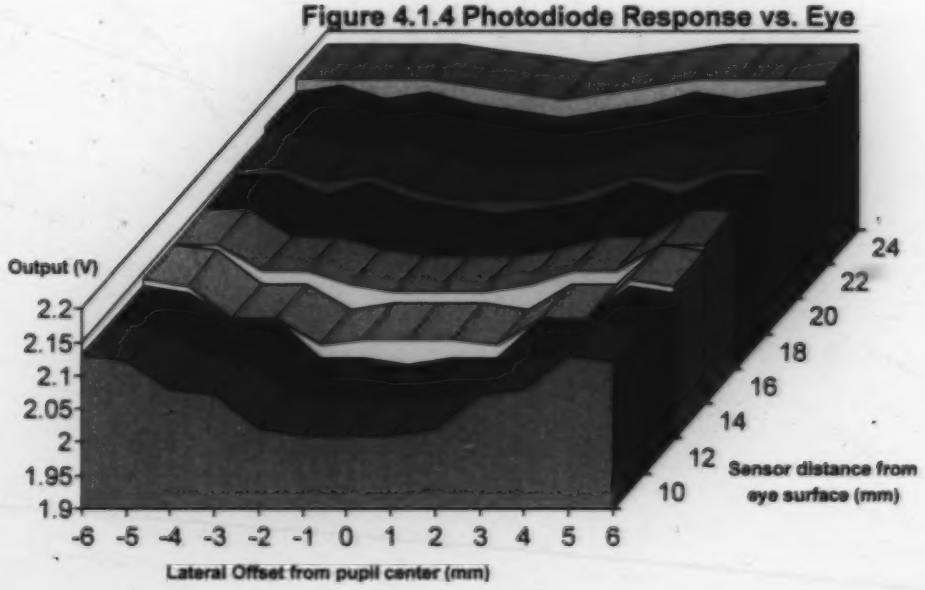


Figure 4.1.3 Prototype Photodiode Test Circuit

Figure 4.1.4 Photodiode Response vs. Eye



4.2 Tracking Circuitry Simulation

The tracking circuitry is perhaps the most simple to test, or rather simulate. However, the results of the simulation are only valid if the models used to represent the circuit are valid. It was necessary to represent three integrated circuits with models of a "make shift" variety. The photodiode, servomotor and both analog multiplexer models are not found within the Electronics Workbench application. With the exception of the servomotor, the above are modeled within the Electronics Workbench application. Several simulations were performed during the course of the design phase. The results of these simulations quickly lead to the completion of the design. Nine such simulations were paramount. The results of these simulations are outlined within this section. These simulations include the photodiode, clock, each of the analog multiplexers, the counting circuit, the register circuit, the comparator and the tracking circuit as a whole.

The first simulation is somewhat trivial. The light conditions to which the photodiode sensors are subject to at any given moment may be represented within the tracking circuitry as static resistor values. As demonstrated in section 4.1, the resistance of the reversed biased

photodiode range between 80kΩ and 1.5MΩ in light conditions ranging between 100W/m^2 and 2W/m^2. The resistor value is incremented to simulate the photodiode response to limited incident light. Conversely, the resistor value is reduced to simulate the photodiode response to brighter incident light. Figure 4.2.1 illustrates the photodiode sensors and the input resistive network.

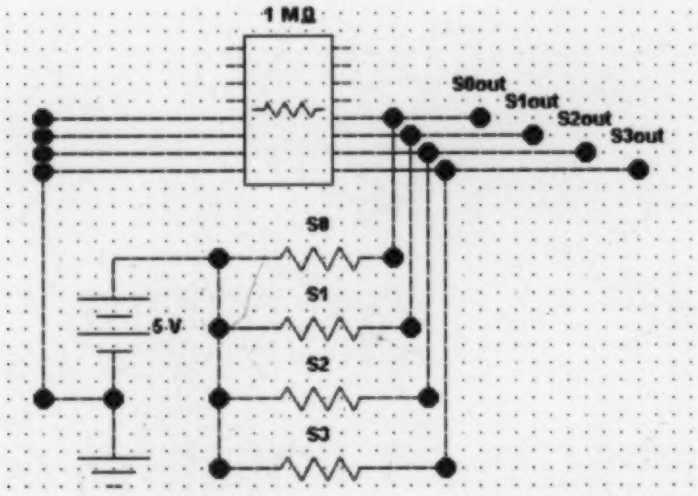


Figure 4.2.1 Photodiode Resistive Simulation Circuit

The clock is connected within the Electronics Workbench application as a standalone circuit as seen in Figure 4.2.2. The periodicity and duty cycle of the output waveforms are represented in Figures 4.2.3.a-d. Most timer implementations are not complex. However, the basic

requirement of a 5% to 7% duty cycle adds a challenge. Clock simulation is important to determine the variation in the period for each resistor set point. In practice the this clock is highly temperature sensitive. To maintain the 20ms clock period to within 10%, the diodes must operate between 0°C and +38°C. This result is verified during the simulation.

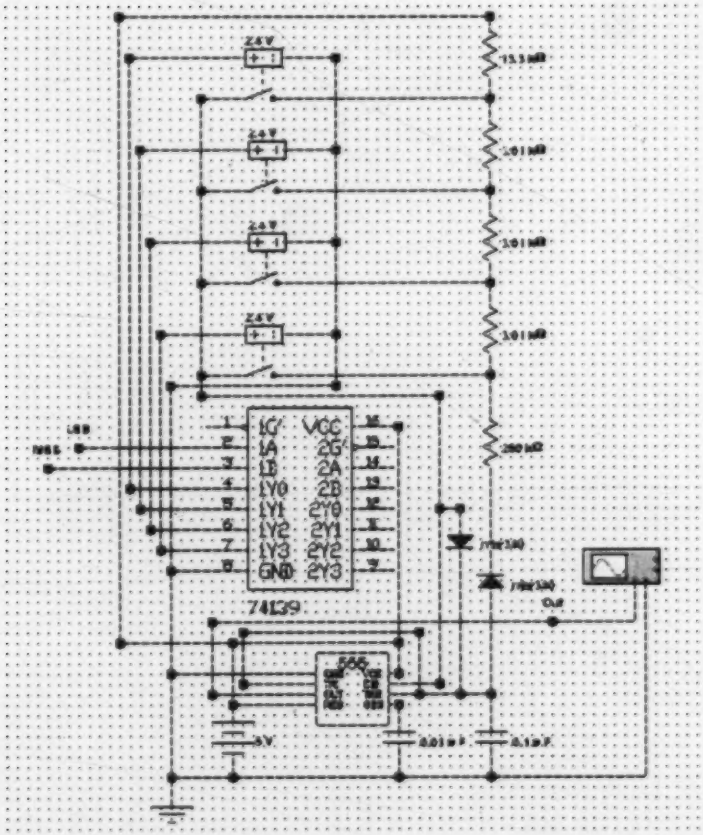


Figure 4.2.2 Prototype Clock Simulation Circuit

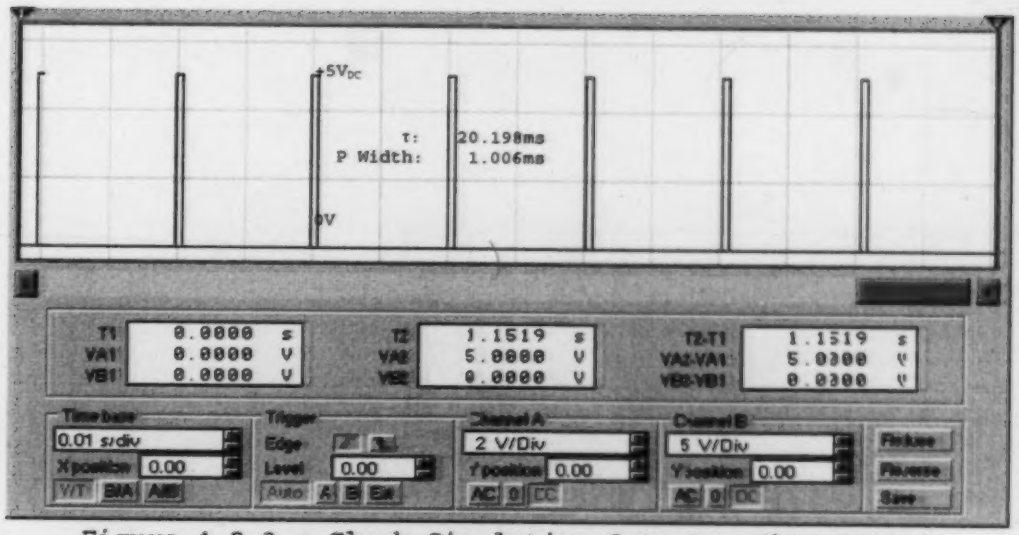


Figure 4.2.3.a Clock Simulation Output - 0b00 Input

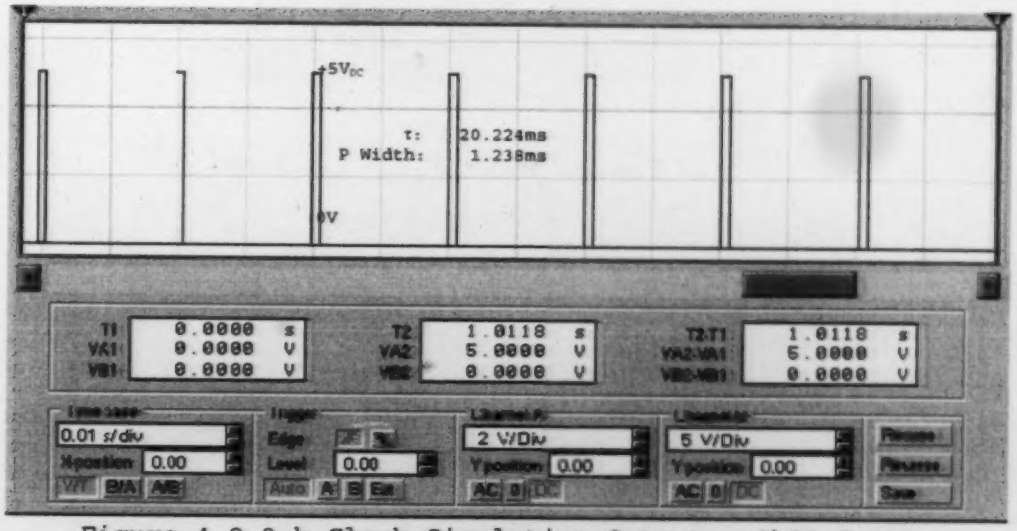


Figure 4.2.3.b Clock Simulation Output - 0b01 Input

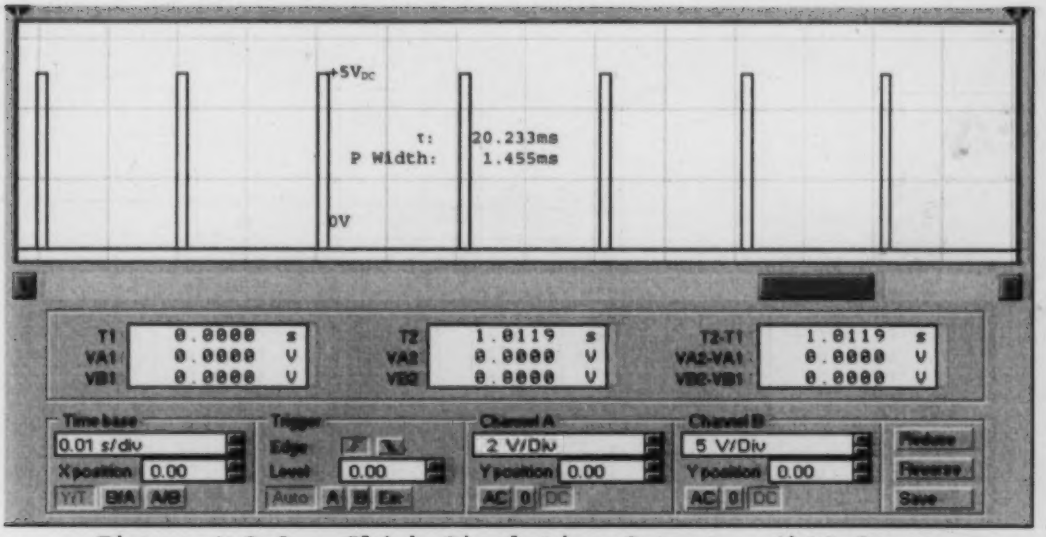


Figure 4.2.3.c Clock Simulation Output - 0b10 Input

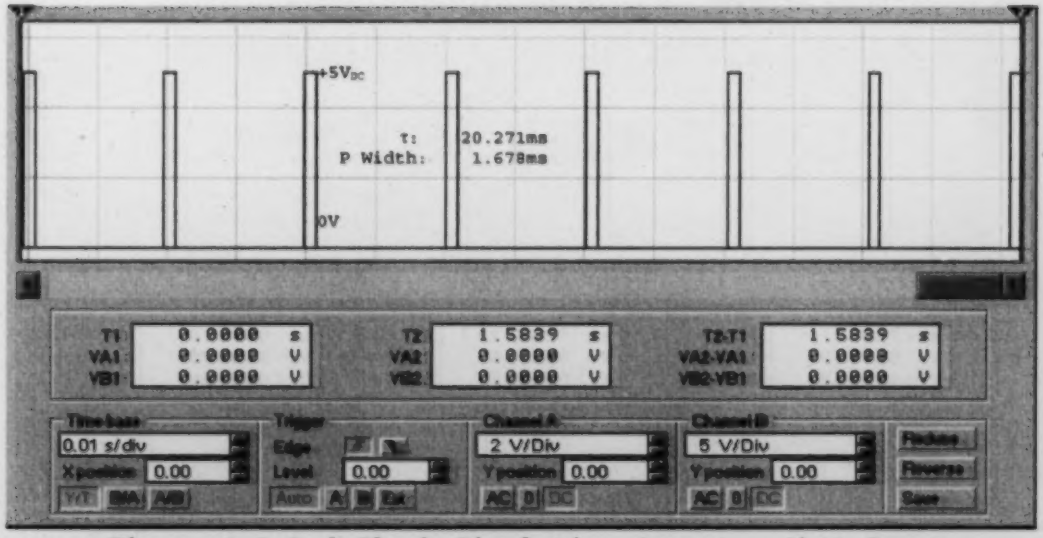


Figure 4.2.3.d Clock Simulation Output - 0b11 Input

Schematically, each of the three analog multiplexers may be represented as a 2-to-4 demultiplexer connected to four voltage-controlled switches. This model is completely accurate. Switch resistor values and logic thresholds of the analog multiplexers are represented in the Electronics Workbench application. Figure 4.2.4 demonstrates the Electronics Workbench representation of the single analog multiplexer. The animated simulation within Electronics Workbench accurately illustrates the changing condition of the voltage-controlled switches during simulation.

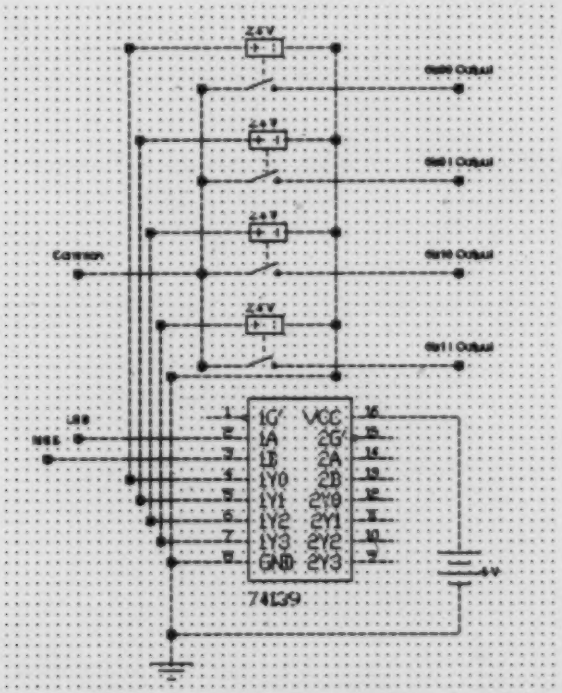


Figure 4.2.4 Prototype Analog Multiplexer

The counting circuit is a single integrated circuit modeled with a 7493 binary counter within the Electronics Workbench application. The 7493 model and the 5493 are identical in all respects except the thermal characteristics. The operation of the counting circuit is verified by connecting light emanating diodes (LED) to the outputs of the counter circuit. While simulating other aspects of the controller, the two animated LEDs indicate the progressive state of the counter at any given time. Figure 4.2.5 illustrates the counter and the LEDs.

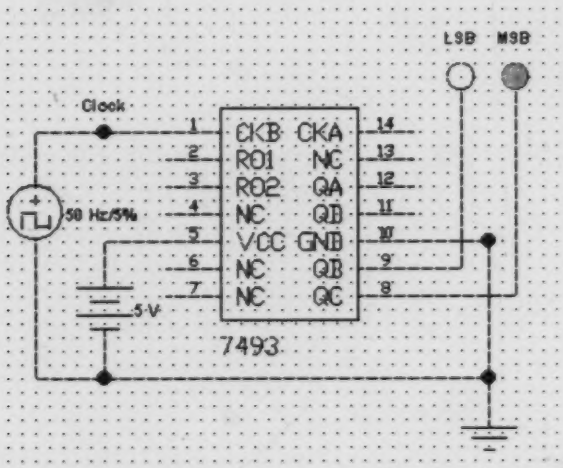


Figure 4.2.5 Prototype Counter Simulation Circuit

The register circuit operation is simulated much like the counter. Like the counter circuit, the register circuit is a single integrated circuit. The register is modeled with a 74194 universal shift register within the Electronics Workbench application. Like the counter, the 74194 model and the 54194 are identical in all respects except the thermal characteristics. The operation of the register circuit is verified by connecting LEDs to the inputs and outputs of the register circuit. Input to the register happens to be the counter output. The animated LEDs indicate the state of the register at all times. Figure 4.2.6 illustrates the register and the LEDs.

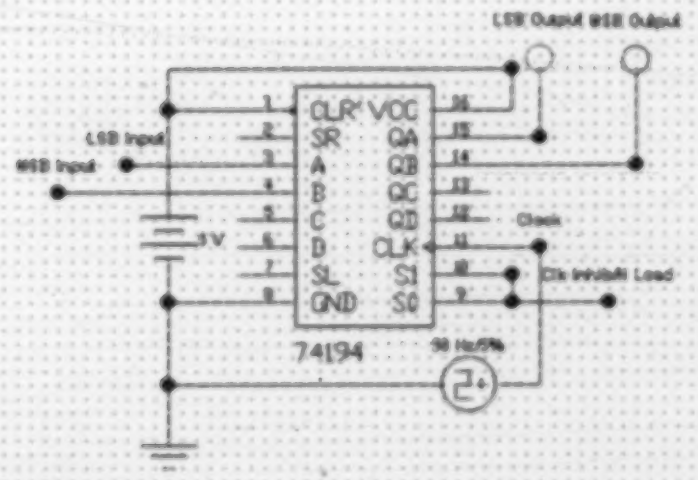


Figure 4.2.6 Prototype Register Simulation Circuit

Time was required to simulate many comparators until just the right comparator model was found. The Maxim MAX975 comparator proved to have the most desirable characteristics of those comparators tested within the application. To critique the comparators, four standard tests were devised to simulate the operational response of the comparators in an environment similar to the operating conditions within the prosthetic controller circuit. Electronics Workbench was set up as in Figure 4.2.7. Two reference voltages (+1V_{DC} and +4V_{DC}) are in connected to both comparator terminals in four simulations.

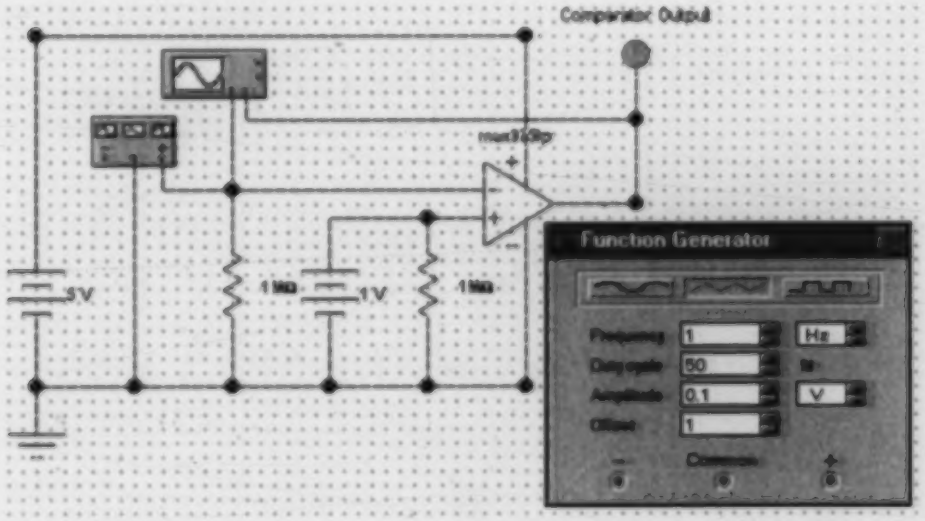


Figure 4.2.7 Comparator Simulation Circuit

The function generator, connected to the alternate input terminal, oscillates a low-frequency triangular waveform about the reference. Results of the simulations for the Maxim MAX975 comparator are depicted in Figures 4.2.8.a through 4.2.8.d.

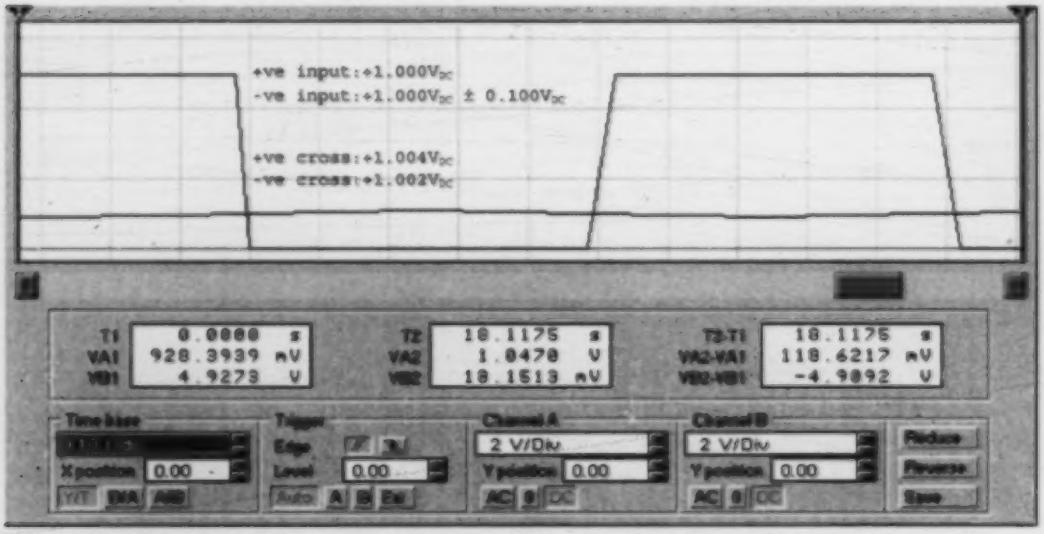


Figure 4.2.8.a Comparator Simulation +ve in at 1V$_{DC}$

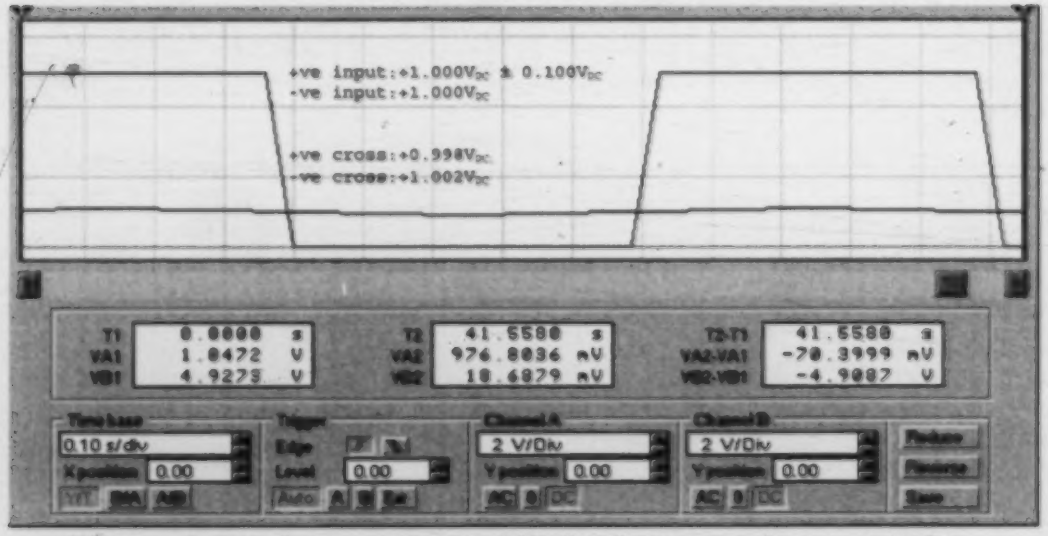


Figure 4.2.8.b Comparator Simulation: -ve in at 1 Volt

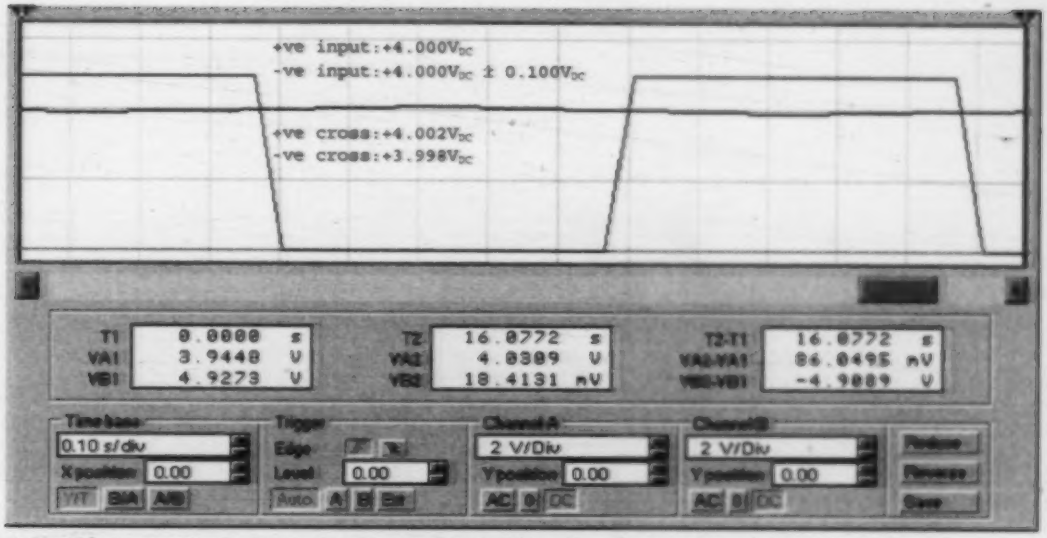


Figure 4.2.8.c Comparator Simulation +ve in at $+4V_{DC}$

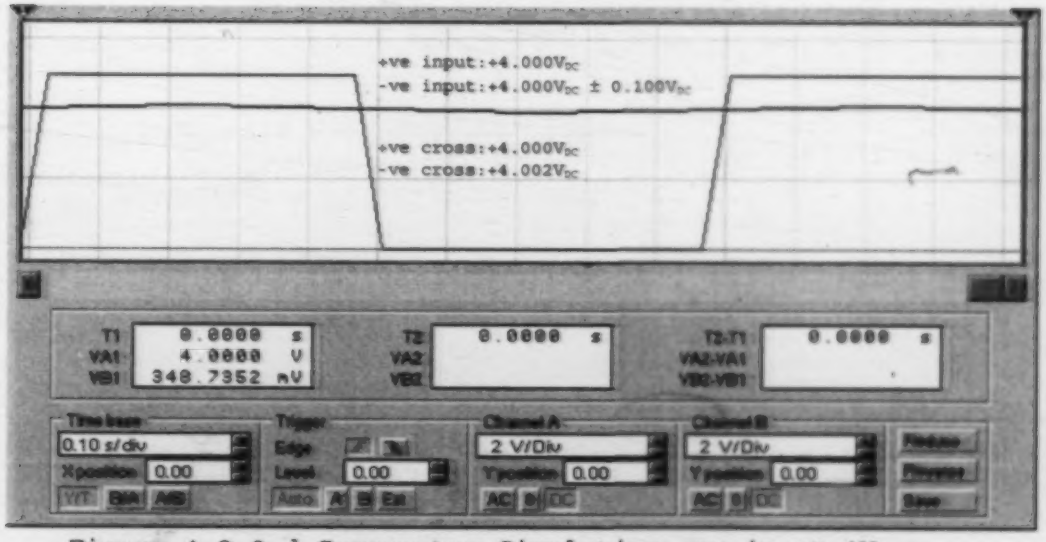


Figure 4.2.8.d Comparator Simulation -ve in at $4V_{DC}$

The final simulation required of the Electronics Workbench application has each sub-circuit working in harmony as a complete tracking controller. The schematic described in section 3.1.3 in Figure 3.1.3.1 is the full circuit. The simulations test the ability of the controller to operate as per the design's intention. Each sensor, modeled with a resistor, takes a sequence of values intended to simulate all 24 unique combinations of sensor states. Sensors S0, S1, S2, and S3 can take a value "1", "2", "3" or "4". Value "1" is the lowest resistive value, value "2" is greater than "1", "3" is greater than "2" and "4" is greater than "3". The sensor with the lowest resistive value, "1", is the sensor which best describes the position of the pupil. The address of value "1" should always be the output of the register after this address is compared to the previous lowest sensor value. State times T0 through T8 are shown. At time "T3", all sensors will be compared. At this time the register output should be unchanged. Table 4.2.9 provides the initial sensor state combinations and the results of the time simulations. The tracking controller register output is correct for all possible sensor input states and the output from the clock is constant after "T3" as per the design intention.

Table 4.2.9 Sensor State Combinations and Register Output

S0	S1	S2	S3	I0	I1	I2	I3	I4	I5	I6	I7	I8
1	2	3	4	00	00	00	00	00	00	00	00	00
1	2	4	3	00	00	00	00	00	00	00	00	00
1	3	2	4	00	00	00	00	00	00	00	00	00
1	3	4	2	00	00	00	00	00	00	00	00	00
1	4	2	3	00	00	00	00	00	00	00	00	00
1	4	3	2	00	00	00	00	00	00	00	00	00
2	1	3	4	00	01	01	01	01	01	01	01	01
2	1	4	3	00	01	01	01	01	01	01	01	01
2	3	1	4	00	00	10	10	10	10	10	10	10
2	3	4	1	00	00	00	11	11	11	11	11	11
2	4	1	3	00	00	10	10	10	10	10	10	10
2	4	3	1	00	00	00	11	11	11	11	11	11
3	1	2	4	00	01	01	01	01	01	01	01	01
3	1	4	2	00	01	01	01	01	01	01	01	01
3	2	1	4	00	01	10	10	10	10	10	10	10
3	2	4	1	00	01	01	11	11	11	11	11	11
3	4	1	2	00	00	10	10	10	10	10	10	10
3	4	2	1	00	00	10	11	11	11	11	11	11
4	1	2	3	00	01	01	01	01	01	01	01	01
4	1	3	2	00	01	01	01	01	01	01	01	01
4	2	1	3	00	01	10	10	10	10	10	10	10
4	2	3	1	00	01	01	11	11	11	11	11	11
4	3	1	2	00	01	10	10	10	10	10	10	10
4	3	2	1	00	01	10	11	11	11	11	11	11

4.3 Servomotor Experimentation

The prosthetic tracking electronics is able to produce exactly four output signals. The encoded control signals are sent by the clock and received by the actuator. Other than by experimentation, there is no other way to ensure that the control signals do indeed produce the desired actuator output. Two experiments are completed to test the operation of the servo and servo electronics. The first experiment tests that the servo is able to produce the desired output in controlled conditions. The second experiment tests the servo's position feedback system by varying the load on the actuator. The servo system should produce the desired output position for various loads.

In the first experiment, a clock circuit as in Figure 4.2.2 is connected. The two analog multiplexer digital inputs can take four unique states. The states are set by manually connecting the leads to ground or to the $+5V_{DC}$ voltage source. The servomotor is wired to the $+5V_{DC}$ voltage source, ground, and the clock output. The actuator position changes as the digital connections to the analog multiplexer change. Relative to a "0" position, defined when the analog multiplexer has value 0b00, each unique digital input combination produces a unique delta position. Value 0b01 causes the actuator to be displaced by

approximately 2mm relation to the "0" position. Value 0b10 causes the actuator to be displaced by approximately 5mm relative to the "0" position. Finally, value 0b11 causes the actuator to be displaced by approximately 7mm. The actuator uses half of the full range of the actuator. Furthermore, the servo-electronics do not seem to be affected by the slight variance in the clock period.

The final experiment is identical to the previous experiment with the addition of one parameter. This experiment attempts to establish that the servomotor employs a position feedback loop and that the actuator can indeed operate while reasonably loaded. Figure 4.2.10 illustrates the experiment.

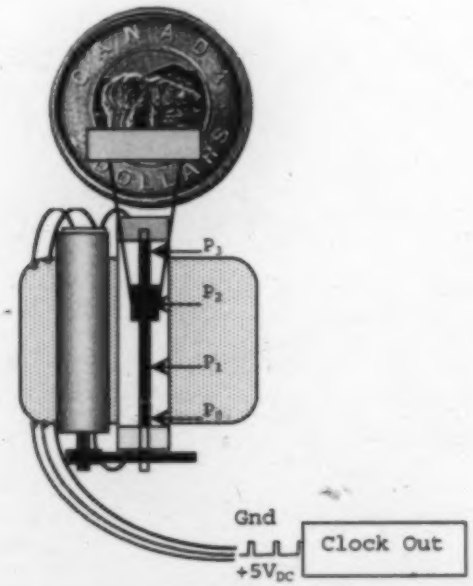


Figure 4.2.10 Loaded Actuator Experiment

The servomotor is loaded by adding weight to the actuator. In all cases, the servomotor is able to produce the desired position. Even by applying a finger on top of the weight and suddenly removing the finger, the actuator slightly overshoots the desired position, and returns to the correct location. This is indeed a position feedback enabled servomotor. The servomotor position feedback system should allow the prosthetic eye controller to operate in a wide variety of loaded states, all the while producing the correct output.

5. Conclusion and Suggestions for Future Research

5.1 Conclusion

The successful design of a discrete lateral position prosthetic eye controller was completed. This non-invasive prosthetic eye controller uses discrete analog, mixed and digital integrated circuit components including infrared sensors, a clock, counter, register, analog multiplexers, a comparator, servo and servo electronics. The position of the eye is determined from four infrared sensors that detect light reflected from within the eye. Control signals are sent to a servomotor decoder within the optical cavity. The control signals sent to the prosthesis result in a controlled bi-directional stepped lateral pivot of the prosthesis about the vertical axis of its rotation.

The lateral position prosthetic eye controller has the following features: (1) Hardware components are selected based upon returning a cosmetically pleasing design. (2) Tight integration and circuit function sharing reduce controller circuit size. (3) Custom designed eye position tracking circuitry minimizes the number of clock cycles required to collect sensor data. This reduces the actuator lag. (4) Four discrete actuator output states maintain controller stability and minimize the perceived position

errors. (5) The custom design provides a non-invasive, discrete, lateral position prosthetic eye controller prototype to the research world. A production ready version of this design can be built with minimal cost and time.

5.2 Suggestions for Future Research

The present lateral position eye controller has a limited operational capacity. While an advanced prosthetic design can benefit from the foundation of the research performed, there are several recommended design changes that should be considered. Recommended design changes include: (1) An increase in the number of sensors in both the lateral and vertical directions. (2) Design of velocity sensitive tracking and a variable speed servo. (3) Design of a controller able to filter or process the physiology of the blink. (4) Implementation of low voltage surface mount integrated circuits. (5) Transfer of the controller logic to a micro-controller. (6) Design of a self-contained optical prosthesis, such that external leads are no longer required.

It is recommended that additional tracking sensors be incorporated into the design. The present design uses four infrared sensors. Future designs can benefit by using as

many as sixteen such sensors. This first recommendation will improve the position control of the prosthesis by detecting a greater range of eye movements in the lateral direction and actuating the prosthesis to stop at as many positions. The change should result in a smoother movement of the prosthesis. The 1MΩ sensor resistors can also be tuned to help equalize the measurement differences in distance between the sensors and the reflective surfaces.

A closely related recommendation further increases the dimensional functionally of the prosthesis. Sensors can also be mounted on the glasses at intervals along a vertical line. Additional circuitry would be required to track longitudinal eye movements and a second servo could pivot the prosthesis about the lateral axis of rotation.

The second recommendation would effectively reduce the relative position error of the prosthesis with respect to the human eye. The current servo design allows the servo to operate in two directions at one speed. Velocity sensitive tracking and use of a variable speed servomotor could better allow the prosthesis to move in perfect synchronicity with the human eye during both fast and slow eye movements. Velocity information could be implemented at the controller by regulating the current available to the servo as a function of the human eye velocity.

A third recommended change to the controller would allow the controller the ability to filter or process the physiology of the blink. The controller detects all eye movements. Unfortunately, the blink is not processed or filtered by the controller. The result of the comparison will is of no value to the prosthetic controller. At this time the effect of the blink is overlooked. Future designs should consider processing blink information to either filter the undesirable effects and/or process the blink to actuate an artificial eyelid.

The design attempts to use the best available low power and low profile components. Unfortunately not all of the components described are available in surface mount packages and low voltage single source packages. Ideally the tight integration of surface mount components allows the design to be mounted invisibly on the frame of the glasses. Components requiring a single $+3V_{DC}$ voltage supply would extend the lifetime of the battery.

With additional sensors in lateral and longitudinal directions, an additional position controller, speed and blink processing functionality the size of the prosthetic eye controller circuit quickly escalates. While, analog circuitry is required to condition sensor information, the controller logic of the clock, counter and register can be

consolidated within a single micro-controller. A micro-controller is easily programmed to perform all of the logic that the existing controller performs. Additional functionality is also easily integrated into a micro-controller. A single micro-controller can take on multiple functions while maintaining a manageable circuit size.

The final possibility of extending this project's value relates to designing the prosthesis and the controller as completely self-contained devices. Both the controller and the prosthesis are connected to an external $+9V_{DC}$ battery. A $+9V_{DC}$ battery is not exactly discrete, natural or cosmetic. Ideally, a low-power controller implanted within the body would be completely invisible and life long-lasting. Similarly, an internally powered prosthesis would eliminate the need for external connecting wires. Implant research, while a fascinating possibility, has many new engineering and biomedical concerns. Less than ideal, but far more esthetically pleasing is the simple optical relay of control signals to a self-contained prosthesis. This would allow the glasses to be removed from the face without battery and control wires being connected to the face. The future research possibilities of this project are only limited by the imagination of the engineer.

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A. Appendix: SPICE Netlist

```
* \ewb5\samples\eye_4_channel\thesis_draft_3.ewb *
*  Interactive Image Technologies                *
*                                                *
*  This File was created by:                     *
*    Electronics Workbench to SPICE netlist      *
*    conversion DLL                              *
*                                                *
*  Title:      Prosthetic Eye Controller Model   *
*  Date:       Fri Aug 07 22:43:03 1998          *
*  Drawn By:   Todd Paul Shepel                  *
************************************************

* Battery(s)
*
V2 509 0 DC 5

* Resistor(s)
*
R17 493 509 13.3K
*
R18 494 493 3.01K
*
R19 495 494 3.01K
*
R20 496 495 3.01K
*
R21 497 496 280K
* S3
R15 509 481 660K
```

```
* S2
R13 509 482 640K
* S1
R14 509 483 620K
* S0
R12 509 444 600K

* Capacitor(s)
*
C2 0 489 10n
*
C3 0 500 100n

* Diode(s)
*
D2 499 500 D_motorol2_mbr340
*
D1 500 497 D_motorol2_mbr340

* Voltage-Controlled Switch(s)
*
V_vcsw_S4 480 444 440 0 vcsw_1_5V_1_55V_200_1T
*
V_vcsw_S3 480 483 403 0 vcsw_1_5V_1_55V_200_1T
*
V_vcsw_S2 480 482 402 0 vcsw_1_5V_1_55V_200_1T
*
V_vcsw_S1 480 481 389 0 vcsw_1_5V_1_55V_200_1T
*
V_vcsw_S5 444 484 428 0 vcsw_2_4V_2_45V_60_1T
*
V_vcsw_S6 483 484 427 0 vcsw_2_4V_2_45V_60_1T
```

```
*
V_vcsw_S7 482 484 426 0 vcsw_2_4V_2_45V_60_1T
*
V_vcsw_S8 481 484 425 0 vcsw_2_4V_2_45V_60_1T
*
V_vcsw_S10 493 499 498 0 vcsw_2_4V_2_45V_60_1T
*
V_vcsw_S11 494 499 491 0 vcsw_2_4V_2_45V_60_1T
*
V_vcsw_S12 495 499 492 0 vcsw_2_4V_2_45V_60_1T
*
V_vcsw_S9 496 499 490 0 vcsw_2_4V_2_45V_60_1T

* 5-Terminal Opamp(s)
*
X_opamp5_0 484 480 509 0 474 maxim_max975lp

* Connector(s)
* node = 0, label =
* node = 24, label =
* node = 26, label =
* node = 28, label =
* node = 23, label =
* node = 22, label =
* node = 21, label =
* node = 19, label =
* node = 22, label =
* node = 21, label =
* node = 19, label =
* node = 0, label =
* node = 0, label =
* node = 23, label =
```

```
* node = 0, label =
* node = 6, label =
* node = 7, label =
* node = 8, label =
* node = 27, label =
* node = 0, label =
* node = 0, label =
* node = 9, label =
* node = 0, label =
* node = 0, label =
* node = 31, label =
* node = 20, label =
* node = 20, label =
* node = 20, label =
* node = 24, label =
* node = 26, label =
* node = 27, label =
* node = 8, label =
* node = 7, label =
* node = 8, label =
* node = 9, label =
* node = 25, label =
* node = 7, label =
* node = 0, label =
* node = 0, label =
* node = 0, label =
* node = 0, label =
* node = 25, label =
* node = 25, label =
* node = 28, label =
* node = 6, label =
* node = 30, label =
```

```
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* node = 25, label =
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* node = 29, label =
* node = 31, label =
* node = 31, label =
* node = 3, label =
* node = 4, label =
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* node = 4, label =
* node = 3, label =
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* node = 29, label =
* node = 30, label =
* node = 2, label =
* node = 20, label =
* node = 1, label =
* node = 1, label =
* node = 0, label =
* node = 1, label =
* node = 3, label =
* node = 4, label =
* node = 2, label =
* node = 2, label =
* node = 2, label =
* node = 0, label =
* node = 0, label =
* node = 10, label =
* node = 13, label =
* node = 17, label =
* node = 15, label =
```

```
* node = 0, label =
* node = 0, label =
* node = 12, label =
* node = 1, label =
* node = 12, label =
* node = 0, label =
* node = 10, label =
* node = 12, label =
* node = 11, label =
* node = 12, label =
* node = 14, label =
* node = 0, label =
* node = 18, label =
* node = 15, label =
* node = 0, label =
* node = 16, label =
* node = 12, label =
* node = 12, label =
* node = 0, label =
* node = 13, label =
* node = 17, label =
* node = 1, label =
* node = 0, label =
* node = 0, label =
* node = 0, label =
* node = 3, label =
* node = 30, label =
* node = 31, label =
* node = 1, label =
* node = 5, label =
* node = 1, label =
* node = 5, label =
```

```
* node = 1, label =
* node = 2, label =
* node = 2, label =
* node = 0, label =
* node = 12, label =
* node = 12, label =
* node = 5, label =
* node = 0, label =
* node = 33, label =
* node = 1, label =
* node = 12, label =
* node = 5, label =
* node = 5, label =
* node = 5, label =
* node = 2, label =
* node = 1, label =
* node = 0, label =
* node = 0, label =
* node = 0, label =
* node = 0, label =
* node = 30, label =
* node = 30, label =
* node = 31, label =
* node = 0, label =
* node = 30, label =
* node = 31, label =
* node = 0, label =
* node = 1, label =
* node = 1, label =
* node = 31, label =
* node = 30, label =
* node = 1, label =
```

```
* node = 0, label =
* node = 25, label =
* node = 20, label =
* node = 4, label =
* node = 1, label =
* node = 7, label =
* node = 8, label =
* node = 9, label =
* node = 6, label =
* node = 6, label =
* node = 7, label =
* node = 8, label =
* node = 9, label =
* node = 1, label =
* node = 1, label =
* node = 1, label =
* node = 1, label =
* node = 1, label =
* node = 9, label =

* 555 Timer(s)
*
X555_U73 0 500 502 509 489 500 499 509 555

* Resistor Pack(s)
*
XRESPK_R16 OPEN_10 OPEN_11 OPEN_12 OPEN_13 0 0 0 0 OPEN_14
OPEN_15 OPEN_16
+OPEN_17 444 483 482 481 RESPK
Roc_OPEN_10 OPEN_10 0 1Tohm
Roc_OPEN_11 OPEN_11 0 1Tohm
Roc_OPEN_12 OPEN_12 0 1Tohm
```

```
Roc_OPEN_13 OPEN_13 0 1Tohm
Roc_OPEN_14 OPEN_14 0 1Tohm
Roc_OPEN_15 OPEN_15 0 1Tohm
Roc_OPEN_16 OPEN_16 0 1Tohm
Roc_OPEN_17 OPEN_17 0 1Tohm

* Red Probe(s)
* red
.PROBE D(PrbR506)
UPrbR_U77 BUF $G_DPWR $G_DGND 506 PrbR506 D0_GATE IO_STD
* red
.PROBE D(PrbR504)
UPrbR_U76 BUF $G_DPWR $G_DGND 504 PrbR504 D0_GATE IO_STD

* 74194 (4-bit Bidirectional Univ. Shift Reg)(s)
*
X74194_1_U69 502 509 474 474 OPEN_18 OPEN_19 505 503
OPEN_20 OPEN_21 506
+504 OPEN_22 OPEN_23 74194
R74194_U69 509 0 200
Uoc_OPEN_18 BUF $G_DPWR $G_DGND $D_LO OPEN_18 D0_GATE
IO_STD
Uoc_OPEN_19 BUF $G_DPWR $G_DGND $D_LO OPEN_19 D0_GATE
IO_STD
Uoc_OPEN_20 BUF $G_DPWR $G_DGND $D_LO OPEN_20 D0_GATE
IO_STD
Uoc_OPEN_21 BUF $G_DPWR $G_DGND $D_LO OPEN_21 D0_GATE
IO_STD
Uoc_OPEN_22 BUF $G_DPWR $G_DGND $D_LO OPEN_22 D0_GATE
IO_STD
Uoc_OPEN_23 BUF $G_DPWR $G_DGND $D_LO OPEN_23 D0_GATE
IO_STD
```

```
* 7493 (4-bit Binary Counter)(s)
*
X7493A_1_U71 OPEN_3 502 OPEN_1 OPEN_2 OPEN_4 505 503 OPEN_5
7493A
R7493_U71 509 OPEN_6 200
Uoc_OPEN_1 BUF $G_DPWR $G_DGND $D_LO OPEN_1 D0_GATE IO_STD
Uoc_OPEN_2 BUF $G_DPWR $G_DGND $D_LO OPEN_2 D0_GATE IO_STD
Uoc_OPEN_3 BUF $G_DPWR $G_DGND $D_LO OPEN_3 D0_GATE IO_STD
Uoc_OPEN_4 BUF $G_DPWR $G_DGND $D_LO OPEN_4 D0_GATE IO_STD
Uoc_OPEN_5 BUF $G_DPWR $G_DGND $D_LO OPEN_5 D0_GATE IO_STD
Uoc_OPEN_6 BUF $G_DPWR $G_DGND $D_LO OPEN_6 D0_GATE IO_STD
Uoc_OPEN_7 BUF $G_DPWR $G_DGND $D_LO OPEN_7 D0_GATE IO_STD
Uoc_OPEN_8 BUF $G_DPWR $G_DGND $D_LO OPEN_8 D0_GATE IO_STD
Uoc_OPEN_9 BUF $G_DPWR $G_DGND $D_LO OPEN_9 D0_GATE IO_STD

* 74139 (Dual 2-to-4 Dec/DEMUX)(s)
*
X74LS139A_1_U58 0 505 503 440 403 402 389 74LS139A
X74LS139A_2_U58 OPEN_32 506 504 428 427 426 425 74LS139A
R74139_U58 509 0 200
Uoc_OPEN_32 BUF $G_DPWR $G_DGND $D_LO OPEN_32 D0_GATE
IO_STD
*
X74LS139A_1_U72 OPEN_24 506 504 498 491 492 490 74LS139A
X74LS139A_2_U72 OPEN_25 OPEN_27 OPEN_26 OPEN_28 OPEN_29
OPEN_30 OPEN_31
+74LS139A
R74139_U72 509 0 200
Uoc_OPEN_24 BUF $G_DPWR $G_DGND $D_LO OPEN_24 D0_GATE
IO_STD
```

```
Uoc_OPEN_25 BUF $G_DPWR $G_DGND $D_LO OPEN_25 D0_GATE
IO_STD
Uoc_OPEN_26 BUF $G_DPWR $G_DGND $D_LO OPEN_26 D0_GATE
IO_STD
Uoc_OPEN_27 BUF $G_DPWR $G_DGND $D_LO OPEN_27 D0_GATE
IO_STD
Uoc_OPEN_28 BUF $G_DPWR $G_DGND $D_LO OPEN_28 D0_GATE
IO_STD
Uoc_OPEN_29 BUF $G_DPWR $G_DGND $D_LO OPEN_29 D0_GATE
IO_STD
Uoc_OPEN_30 BUF $G_DPWR $G_DGND $D_LO OPEN_30 D0_GATE
IO_STD
Uoc_OPEN_31 BUF $G_DPWR $G_DGND $D_LO OPEN_31 D0_GATE
IO_STD

* Misc
.MODEL D_motorol2_mbr340 D(Is=720.356n Rs=29.2105m
Cjo=496.118p
+Vj=475.291m Tt=400n M=440.738m BV=52 N=1.03833 EG=600m
XTI=3.135 KF=0
+AF=1 FC=500m IBV=10m TNOM=27)

.MODEL vcsw_1_5V_1_55V VSWITCH(Von=1.5 Voff=1.55 Ron=200)

.MODEL vcsw_2_4V_2_45V VSWITCH(Von=2.4 Voff=2.45 Ron=60)

.SUBCKT maxim_max975lp   1 2 3 4 97
*
  f101     3  9 v1 1
  Iee100    7  400 dc 100.0E-6
  q101     9  20  7 qin
  Q2     8  21  7 qin
```

```
  Q3    9  8  399 qmo
  Q4    8  8  399 qmi
  VMB 400 4 0V
  VPB 399 3 0V
***=================
VIN1 2 23 .95
VIN2 1 25 .95
***
IPSUP 3 0 -100ua
INSUP 0 4 -100ua
***
EHYST 23 20 POLY(1) 0 60 0 1
VS2 21 25 0V
.model qin NPN(Is=800.0E-18 Bf=10000)
.model qmi PNP(Is=800.0E-18 Bf=1002)
.model qmo PNP(Is=800.0E-18 Bf=1000 Cjc=1E-15 Tr=298.1E-9)
.MODEL PMOS PMOS
*(VTO=-1.7 KP=1.8E-3)
  e1   10  4  3  9  2
  v1   10 11 dc 0
  q5    5 11  44 qoc
  vshift 44 4 0v
  *clamps output, Q5 collector load.
  R55 3 5 1meg
  DP5 5 3 DP
  DP6 4 5 DP
***============= Hysterisis section
GH 0 51 97 101 1E-6
ECM 101 0 3 4 0.5
RCM 101 0 1MEG
****==============COMPARATOR POINT FOR CREATING LOGIC
OUTPUT, +-1, hi,lo.
```

```
RH1 3 51 1E11
RH2 4 51 1E11
DP1 51 52 DP
DP2 53 51 DP
VP1 52 0 1V
VP2 53 0 -1V
***=================
IHYST 55 0 -2E-9
*GENERATES 2MV OF HYST.
RREF 55 0 1E6
*LOGIC OUTPUT, NODE 60 ALTERS THE POLARITY, SO 55 SHOULD
ALWAYS BE POS.
GMULT 60 0 POLY(2) 51 0 55 0 0 0  0 0 1E-6
RMULT 60 0 1E6
*=================
*EH 3 98 3 4 0.5
VVIRTUAL 98 0 0V
F5 3 38 VA8 1
D9 40 38 DX
D10 38 3 DX
VA7 3 40 0
F6 3  4 VA7 1
G12 98 32 5 0 7.04E-3
R15 98 32 140
D3 36 41 DP
D4 42 37 DP
V4 37 34 0
V5 34 36 0
***V4,V5 SET ISC, V4 VOL, V5 VOH.
R16 41 35 25
*was 150
R17 42 35 45
```

```
E11 3 33 3 32 1
VA8 33 34 0V
L 35 97 10NH
*=========================
.model qoc NPN(Is=800.0E-18 Bf=10.35E3 Cjc=1E-15 Tf=48.1e-
12 Tr=201.2E-9)
.MODEL DX  D(Is=800.0E-18)
.MODEL DP D(N=0.001)
*=========================
***== MODELS USED ==***
.MODEL DX2 D(IS=1E-15 n=0.001)
*.MODEL DX D(IS=1E-15)
.ENDS

.SUBCKT 555 5 1 3 7 8 2 4 6
    R0 5 16 5K
    R1 16 8 5K
    R2 8 6 5K
    R3 4 15 1
    E0 9  0 VALUE = {IF(V(16, 1)>0, 5, 0)}
    E1 10 0 VALUE = {IF(V(2, 8)>0, 5, 0)}
    S0 5 15 14 0 vcsw2
    S1 3 6 13 0 vcsw1
    UTBUF0 BUF3 $G_DPWR $G_DGND 12 7 13 D0_TGATE IO_STD
    UTBUF1 BUF3 $G_DPWR $G_DGND 11 7 14 D0_TGATE IO_STD
    URS_FF_0 SRFF(1) $G_DPWR $G_DGND
    + $D_HI $D_HI $D_HI 10 9 11 12 D0_GFF IO_STD
.ENDS
.MODEL vcsw2 VSWITCH(Von=4.99998 Voff=10u Ron=1m Roff=1G)
.MODEL vcsw1 VSWITCH(Von=4.5 Voff=500m Ron=1m Roff=1G)
.OPTIONS DIGINITSTATE=0
.LIB
```

```
.SUBCKT RESPK 1 2 3 4 5 6 7 8 16 15 14 13 12 11 10 9
    R0 1 16 1MEG
    R1 2 15 1MEG
    R2 3 14 1MEG
    R3 4 13 1MEG
    R4 5 12 1MEG
    R5 6 11 1MEG
    R6 7 10 1MEG
    R7 8 9 1MEG
.ENDS

.OPTIONS PIVREL=0.002 ITL1=1000 ITL4=50 METHOD=GEAR
.END
```